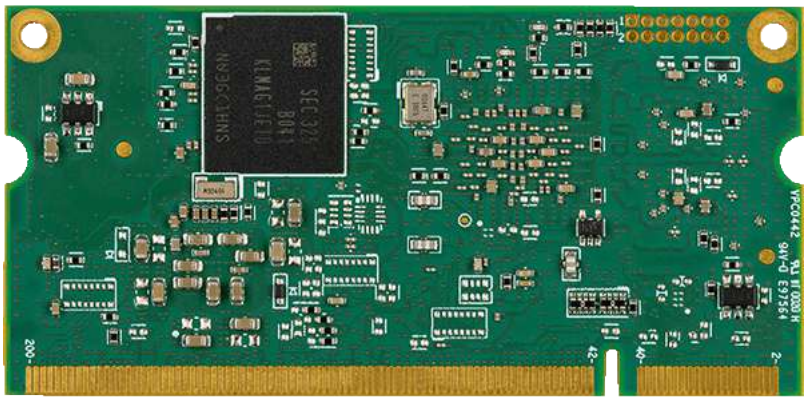
VARISCITE LTD.

VAR-SOM-MX8M-PLUS V2.x Datasheet

NXP i.MX 8M PLUS™ - based System-on-Module



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1. Document Revision History

Revision	Date	Notes
1.0	March 18, 2024	Initial release, updated the below to follow VAR-SOM-MX8M-PLUS Rev2.x design: • Block Diagram • SOM pictures • Pinout/Pinmux tables throughout document for pins: 31,33,35,48,70,72,75,77,82,84,86,117,145,147,173,191 • HW configuration table section 6 • Ethernet, Wi-Fi, uSDHC, TSC sections 5.4,5.6,8.4,8.5,8.6,8.10 • Power consumption section 10.4 • Assembly options section 9 • SOM drawing section 12.3 Removed USB2_OTG_ID alternate (pin 69) per NXP reference manual Rev 2 update

2. Table of Contents

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4. Overview

4.1 General Information

The VAR-SOM-MX8M-PLUS offers a high-performance processing for a low-power System-on-Module.
The product is based on the i.MX 8M Plus family which is a set of NXP products focused on machine learning applications, combining state-of-art multimedia features with high-performance processing optimized for low-power consumption.

The i.MX 8M Plus Media Applications Processor is built to achieve both high performance and low power consumption and relies on a powerful, fully coherent core complex based on a quad Cortex-A53 cluster and Cortex-M7 low-power coprocessor, audio digital signal processor, machine learning and graphics accelerators.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux and an RTOS like FreeRTOS™ on the Cortex-M7 core for time and security critical tasks.

The VAR-SOM-MX8M-PLUS provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Symphony-Board – evaluation board
  - ✓ Carrier Board, compatible with VAR-SOM-MX8M-PLUS
  - ✓ Schematics
- VAR-DVK-MX8MP full development kit, including:
  - ✓ Symphony-Board
  - ✓ VAR-SOM-MX8M-PLUS
  - ✓ Display and touch
  - ✓ Accessories and cables
- O.S support
  - ✓ Linux BSP
  - ✓ Android

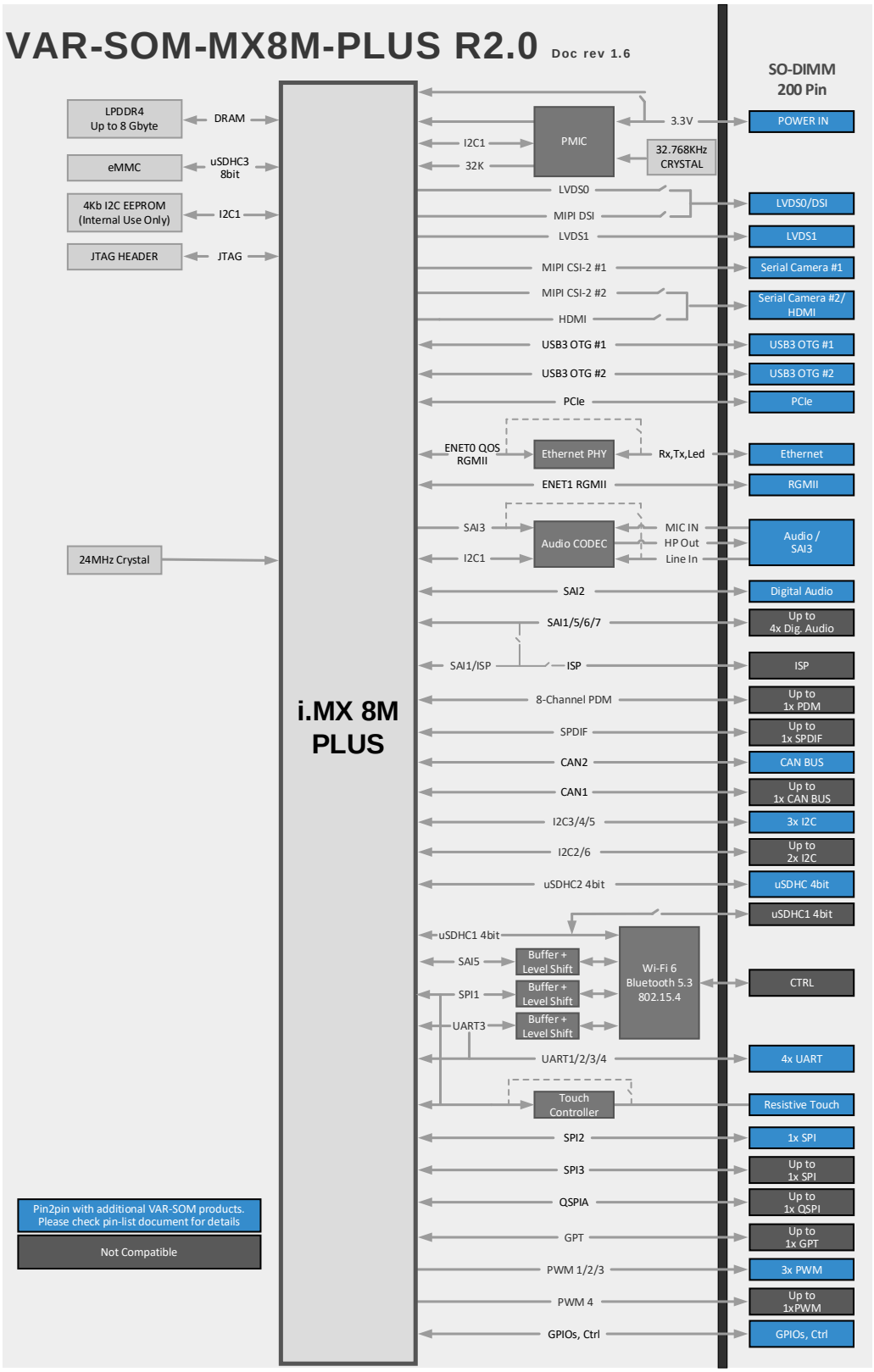
Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- NXP i.MX8M-PLUS series SOC
  - 4x Cortex A53 up to @ 1.8 GHz
  - 1x Cortex M7 @ 800 MHz
  - 1x Hi-Fi DSP @ 800 MHz
- Hardware 2D/3D Graphics Acceleration
  - GC7000UltraLite 3D GPU (2 shaders) OpenGL ES 3.0, OpenCL1.2, Vulkan
  - GC520L 2D GPU
- Machine Learning: NPU (Neural Processing Unit) 2.3 TOPS Neural Network performance
  - Keyword detect, noise reduction, beamforming
  - Speech recognition (i.e. Deep Speech 2)
  - Image recognition (i.e. ResNet-50)
- Memory
  - Up to 8GB LPDDR4 RAM @ 2000Mhz
  - 8-bit up to 128GB eMMC boot and storage
- Display Support
  - 2x LVDS interface 4-lane each
  - HDMI 2.0a
  - 1x MIPI DSI with up to 4 data lanes
- Networking
  - 2x 10/100/1000 Mbit/s Ethernet Interface
  - Certified Wi-Fi 802.11 ac/a/b/g/n
  - Bluetooth: 5.2/BLE
- Camera
  - Up to 2x MIPI CSI – CMOS Serial camera Interface 4 lanes
  - 375 Mpixel/s HDR ISP (Image Sensor Processor)
- Audio
  - Analog Stereo line in
  - Analog headphones out
  - Digital microphone
  - Up to 6x Digital audio (SAI)
  - 8-channel PDM microphone input
  - SPDIF
- USB
  - 2x USB 3.0/2.0 Host/Device
- Other Interfaces
  - SDIO/MMC
  - 1x PCIe v3.0
  - Resistive touch controller
  - Serial interfaces (ECSPI, FlexSPI, I2C, UART, CAN, JTAG)
  - GPIOs
- Single power supply: 3.3V
- Dimensions (W x L x H): 67.6 mm x 33 mm x 3.4 mm
- Industrial temperature range: -40°C to 85°C

4.3 Block Diagram

Figure 1 : VAR-SOM-MX8M-PLUS Block Diagram



5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SOM-MX8M-PLUS.

5.1 NXP i.MX 8M Plus

5.1.1 Overview

The i.MX 8M Plus family focuses on machine learning and vision, advanced multimedia, and industrial IoT with high reliability. It is built to meet the needs of Smart Home, Building, City and Industry 4.0 applications.

- Powerful quad or dual Arm® Cortex®-A53 processor with a Neural Processing Unit (NPU) operating at up to 2.3 TOPS.
- Real-time control with Cortex-M7. Robust control networks supported by dual CAN FD (IT version) and dual Gigabit Ethernet, one of which, with Time Sensitive Networking (TSN).
- The multimedia capabilities include video encode (including h.265) and decode, 3D/2D graphic acceleration, and multiple audio and voice functionalities.
- Dual Image Signal Processors and two camera inputs for an effective Vision System.
- High industrial reliability with DRAM inline ECC and ECC on on-chip RAM.

5.1.2 i.MX 8M Plus Block Diagram

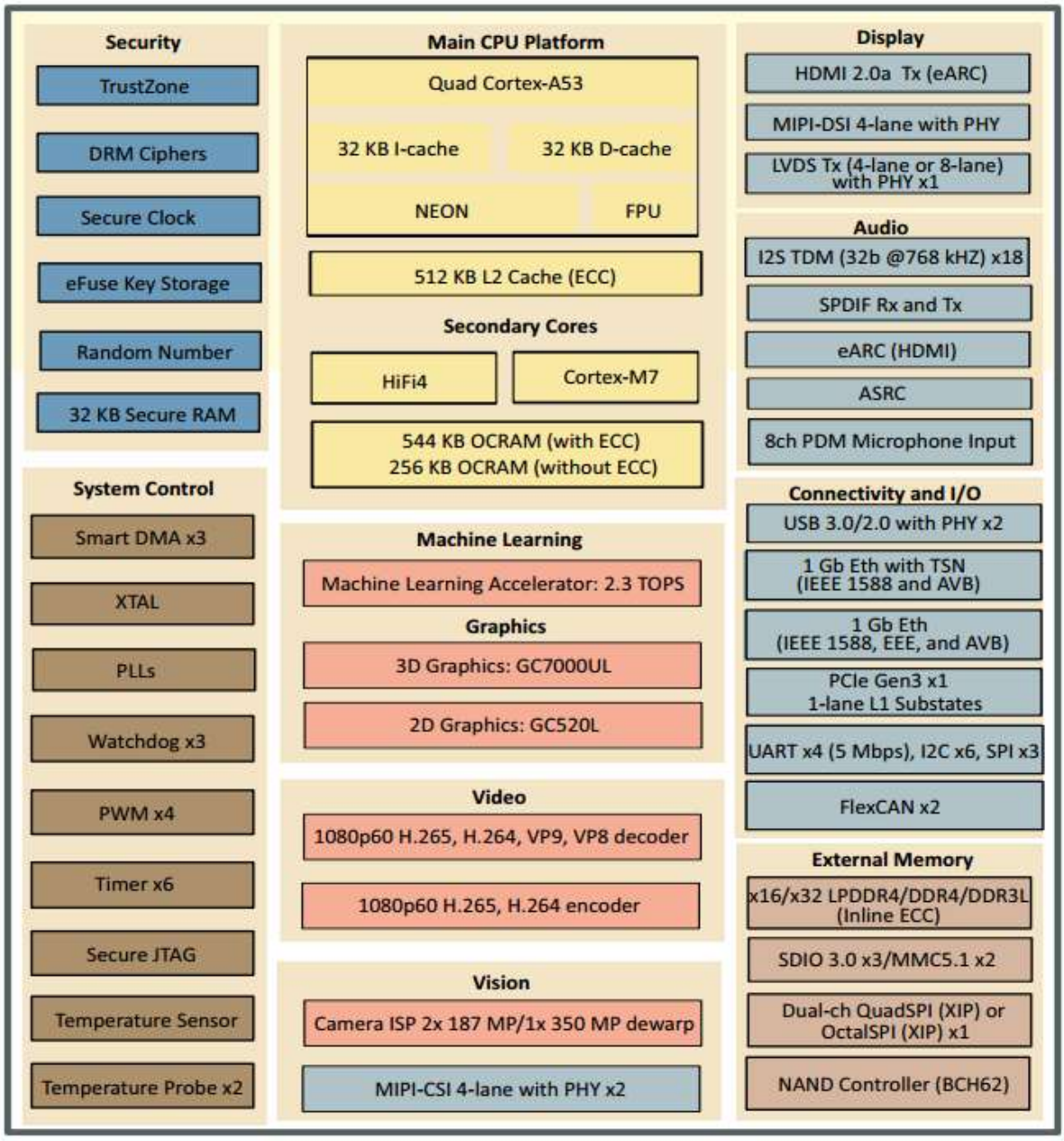


Figure 2 : i.MX 8M Plus Block Diagram

5.1.3 ARM Cortex-A53 MPCore™ Platform

The i.MX 8M Plus family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- Quad symmetric Cortex-A53 processors operation up to 1.8 GHz, including:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit Armv8-A architecture
  512 KB unified L2 cache

5.1.4 Arm Cortex M7 Platform

The Cortex-M7 Core Platform includes the following:

- Low power microcontroller available for customer application:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - 256 KB TCM
- Available customer applications include:
  - Low power standby mode
  - IoT device control
  - ML applications

5.1.5 System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NoC) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

5.1.6 Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
  - Simplified clock tree structure
  - Unified clock programming model for each clock root
  - Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

5.1.7 Interrupts and DMA

Interrupts and DMA include:

- 160 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller GIC) and Cortex-M7 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines
- are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also others peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6/7, SPDIF and PDM audio input

5.1.8 On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-Chip RAM - OCRAM (576KB)
- Audio Processor System RAM - OCRAM_A (256KB)
- On-Chip RAM for State Retention - OCRAM_S (36KB)

5.1.9 External Memory Interface

The external memory interfaces supported on this chip include:

- 32-bit DRAM Interface:
    - LPDDR4-4000
    - DDR4-3200
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.1 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- FlexSPI FLASH with support for XIP (for Cortex-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices

5.1.10 Timers

- The timers on this chip include:
- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M7 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

5.1.11 Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:

• One GPU for 2D and composition acceleration

- Supports multi-source composition
- Supports one-pass filter
- Supports tile format

• One GPU for 3D processing

- Two Shader Execution Units
- Supports OpenGL ES 1.1, 2.0, 3.0, 3.1
- Supports OpenCL 3.0
- Supports OpenVG 1.1
- Supports OpenGL 4.0
- Supports EGL 1.5
- Supports Vulkan 1.1
- Supports tile format

5.1.12 Graphics Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- Video Decode:
  - 1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) (VPU G2)
  - 1080p60 VP9 Profile 0, 2 (VPU G2)
  - 1080p60 VP8 (VPU G1)
  - 1080p60 AVC/H.264 Baseline, Main, High decoder (VPU G1)
- Video Encode:
  - 1080p60 AVC/H.264 encoder
  - 1080p60 HEVC/H.265 encoder
- TrustZone support

5.1.13 Machine Learning: NPU (Neural Processing Unit)

- 2.3 TOP/s Neural Network performance available for user applications
  - Speech recognition (e.g., Deep Speech 2)
  - Image recognition (e.g., ResNet-50)
  - Object detection (e.g., MobileNet-SSD)

5.1.14 Display Interfaces

The chip has the following display support:

- Three LCDIF Display Controllers:
  - One LCDIF drives MIPI DSI
  - One LCDIF drives LVDS Tx
  - One LCDIF drives HDMI Tx
  - Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.
  - Supports 8-bit / 16-bit / 18-bit / 24-bit / 32-bit pixel depth
  - Supports one layer
- MIPI Interface:
  - One 4-lane MIPI DSI interface
  - Two 4-lane MIPI CSI interfaces
- Two 4-lane LVDS interfaces
- ISI (Image Sensor Interface):
  - The ISI is a simple camera interface that supports image processing and transfer
  - via a bus master interface for up to 2 cameras
- Two Camera ISP (Image Signal Processor):
  - When one camera is used, supports up to 12MP@30fps or 4kp45
  - When two cameras are used, each supports up to 1080p80
- HDMI 2.0a
  - HDMI 2.0a Tx supporting one display
    - Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30
- Audio support
  - 32 channel audio output support
  - 1 S/PDIF audio eARC input support

5.1.15 Audio

Audio include the following:

- Audio DSP
- S/PDIF Input and Output, including a Raw Capture input mode
- Six external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1 RX lanes.
- PDM Microphone Interface module which supports up to 8-microphones (4 lanes)
- Asynchronous Sample Rate Converter (ASRC) module which supports:
  - Processing of up to 32 audio channels
  - 4 context groups
  - 8 kHz to 384 kHz sample rate
  - 1/16 to 8x sample rate conversion ratio

5.1.16 General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- One PCI Express (PCIe):
  - Single lane supporting PCIe Gen 3
  - Dual mode operation to function as root complex or endpoint
  - Integrated PHY interface
  - Supports L1 low power substate
- Two USB 3.0 Type C controllers with integrated PHY interface
  - Backwards compatibility with USB 2.0
  - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
  - MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
  - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100 MB/sec
  - Support for SDXC (extended capacity)
- Two Ethernet controllers, capable of simultaneous operation
  - One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
  - One Gigabit Ethernet controller with support for TSN, EEE, Ethernet AVB and IEEE1588
- Two controller area network (FlexCAN) modules, each optionally supporting flexible data rate (FD)
- Four universal asynchronous receiver/transmitter (UART) modules
- Six I2C modules
- Three SPI modules

5.1.17 Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
  - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:
  - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
  - Support Widevine and PlayReady content protection
  - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms
  - Real-time integrity checker (RTIC)
  - DRM support for RSA, AES, 3DES, DES
  - Side channel attack resistance
  - True random number generation (RNG)
  - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including Secure Real Time Clock (SRTC)
- Secure JTAG Controller (SJC)

5.1.18 Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

5.1.19 GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.20 Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

5.1.21 System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M7 CPUs
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

5.2 Memory

5.2.1 RAM

The VAR-SOM-MX8M-PLUS is available with up to 8 GB of LPDDR4-4000 memory.

5.2.2 Non-volatile Storage Memory

The VAR-SOM-MX8M-PLUS is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

5.3 Audio (WM8904)

The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4 Wi-Fi + BT + LR-WPAN

The SOM can be configured either for using one of two Wi-Fi modules based on NXP chipset:

- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module based on NXP IW612 chipset
- 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module based on NXP IW611 chipset

Both realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port or may be ordered with dual antenna ports.
The SOM can be ordered with 802.15.4 low-rate wireless personal area network (LR-WPAN)

Wi-Fi Key Features:

- 1x1 2.4/5 GHz, up to 80 MHz channel
- UL/DL MU-MIMO and OFDMA
- Target Wake Time, Dual Carrier Modulation, Extended Range
- 802.11az accurate ranging
- WPA3 security

Bluetooth Key Features:

- Supports Bluetooth 5.2
- Integrated high power PA up to +20 dBm transmit power
- Full featured Bluetooth baseband
- SCO/eSCO links with hardware accelerated audio signal processing
- Bluetooth LE 2 Mbit/s, Long Range, Advertising Extensions
- LE Audio with Isochronous channels (I2S/PCM)

802.15.4 Key Features:

- IEEE 802.15.4-2015 compliant supporting Thread in 2.4 GHz band
- Integrated high power PA up to +20 dBm transmit power
- Shared transmitter and antenna pin with Bluetooth
- Simultaneous receive with Bluetooth

5.4.1 VAR-SOM-MX8M-PLUS 2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Option

The VAR-SOM-MX8M-PLUS contains Murata's certified high-performance Type 2EL Module based upon the NXP IW612 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.3 + 802.15.4 wireless connectivity.

5.4.2 VAR-SOM-MX8M-PLUS 2.4GHz & 5GHz Wi-Fi® + Bluetooth® Option

The VAR-SOM-MX8M-PLUS contains Murata's certified high-performance Type 2DL Module based upon the NXP IW611 chipset supporting Wi-Fi® 11a/b/g/n/ac/ax + Bluetooth® 5.3 wireless connectivity.

5.5 PMIC

The VAR-SOM-MX8M-PLUS features Dual Freescale/NXP's PCA9450CHN chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 8M Plus series of application processors. The PCA9450CHN regulates power rails required on SOM from a single 3.3V power supply. The PMIC is fully programmable via the I2C interface and associated register map.
Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6 10/100/1000 Mbps Ethernet Transceiver

The SOM features on board an MXL86110C or MXL86110I Integrated Ethernet Transceiver. Key features include:

- 1000BASE-T (IEEE 802.3), 100BASE-TX (IEEE 802.3) and 10BASE-Te (IEEE 802.3)
- Ethernet twisted pair copper cable of category CAT5 or higher
- Low EMI voltage mode line driver with integrated termination resistors
- Transformer less Ethernet for backplane applications
- Auto-Negotiation (ANEG) with extended next page support
- Auto-MDIX and polarity correction
- Auto-Down speed (ADS)
- Energy-Efficient Ethernet (EEE) and power down mode
- Wake-on-LAN (WoL)
- 10k byte jumbo frame support
- RGMII Interface
- An MDIO slave interface supports IEEE 802.3 Clause 22 and Clause 45
- An MDIO interface clock of up to 12.5 MHz
- Three MDIO message frame types: Clause 22, Clause 22 Extended, and Clause 45
- Two fully programmable LEDs

5.7 Resistive Touch Controller (TSC2046)

The VAR-SOM-MX8M-PLUS features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

5.8 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters. This EEPROM is connected to I2C1 bus and intended only for holding the above information. The SOM may not boot if the contents of EEPROM device are corrupted.

6. VAR-SOM-MX8M-PLUS Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SOM-MX8M-PLUS.

Table 1 Hardware Configuration Options

Option	Description
EC	Ethernet PHY assembled on SOM
AC	Audio Codec assembled on SOM
WBD	2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module assembled on SOM
WBE	2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module assembled on SOM Available only when TP option is not assembled [1]
BTPCM	SAI5 balls internally connected to Bluetooth PCM lines [3]
COEX	WCI-2 coexistence management lines exported via SOM connector pins [3]
WBRST	WLAN, Bluetooth, 802.15.4 reset lines exported via SOM connector pins [3]
ANT2	Dual antenna mode. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4 [3]
SDEX	SD1 lines exported via SOM connector pins. Available only when WBD/ WBE option is not assembled [2]
TP	Resistive Touch controller assembled on SOM [1]
DSI	DSI lanes exported via SOM connector pins instead of LVDS0 lanes
CSI2	2nd MIPI-CSI2 serial camera lanes exported via SOM connector pins instead of HDMI lanes
SAI1	CPU SAI1 balls exported via SOM connector pins instead of GPIO1 balls
QSPI	QSPIA lanes exported via SOM connector pins [2]

NOTE

[1] The utilization of the same SPI channel by WBE and TP assembly choices makes it unfeasible to assemble them simultaneously.
[2] Due to shared SOM pins QSPI and SD1 cannot be assembled simultaneously.
[3] This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for a full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SOM-MX8M-PLUS exposes a 200-pin SO-DIMM connector.

- The recommended mating connectors for baseboard interfacing are:
  1. Concraft - 0701A0BE52E
  2. Tyco Electronics -1565917-4

7.2 Wi-Fi & BT Connector

In Modules with Wi-Fi “WB” or “WBD” Configuration - a combined Wi-Fi + BT antenna connector is assembled.

- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes JTAG interface via an optional header.

7.4 VAR-SOM-MX8M-PLUS Connector Pin-out

Table 2: VAR-SOM-MX8M-PLUS J1 Pinout

Pin	Assembly	Pin name	Notes	GPIO	Ball
1	no EC	ENET_TX_CTL	Referenced to pin 36 supply (1.8V/3.3V); On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	GPIO1_IO22	SOC.AF24
1	EC	NC	With "EC" configuration this pin in Not Connected		NC_EC
2		GND	Digital Ground		GND
3	no EC	ENET_TD3	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO18	SOC.AD24
3	EC	ETH0_MDI_A_P	Signal source is Ethernet PHY		MxL86110x.1
4	no EC	ENET_RD0	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO26	SOC.AG29
4	EC	ETH0_MDI_C_P	Signal source is Ethernet PHY		MxL86110x.6
5	no EC	ENET_TD2	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO19	SOC.AF26
5	EC	ETH0_MDI_A_M	Signal source is Ethernet PHY		MxL86110x.2
6	no EC	ENET_RD1	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO27	SOC.AG28
6	EC	ETH0_MDI_C_M	Signal source is Ethernet PHY		MxL86110x.7
7		GND	Digital Ground		GND
8		GND	Digital Ground		GND
9	no EC	ENET_TD1	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO20	SOC.AE26
9		ETH0_MDI_B_P			MxL86110x.4
10	no EC	ENET_RD2	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO28	SOC.AF29
10	EC	ETH0_MDI_D_P	Signal source is Ethernet PHY		MxL86110x.9
11	no EC	ENET_TD0	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO21	SOC.AC25
11	EC	ETH0_MDI_B_M	Signal source is Ethernet PHY		MxL86110x.5
12	no EC	ENET_RD3	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO29	SOC.AF28
12	EC	ETH0_MDI_D_M	Signal source is Ethernet PHY		MxL86110x.10
13		GND	Digital Ground		GND
14		GND	Digital Ground		GND
15	no EC	ENET_RX_CTL	Referenced to pin 36 supply (1.8V/3.3V)	GPIO1_IO24	SOC.AE28
15	EC	ETH0_LED_ACT	Signal source is Ethernet PHY		MxL86110x.32
16	no EC	ENET_RXC	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter	GPIO1_IO25	SOC.AE29
16	EC	ETH0_LED_LINK_10_100_1000	Signal source is Ethernet PHY		MxL86110x.33
17		SPDIF_EXT_CLK		GPIO5_IO05	SOC.AC18
18	no AC	SAI3_TXD	Available in SOM without "AC" configuration	GPIO5_IO01	SOC.AH18
18	AC	DMIC_CLK	Signal source is Audio Codec		WM8904.1
19		GND	Digital Ground		GND
20	no AC	SAI3_MCLK	Available in SOM without "AC" configuration	GPIO5_IO02	SOC.AJ20
20	AC	DMIC_DATA	Signal source is Audio Codec		WM8904.27
21		SAI2_RXD0		GPIO4_IO23	SOC.AJ14
22		SAI2_RXC		GPIO4_IO22	SOC.AJ16
23		SAI2_RXFS		GPIO4_IO21	SOC.AH17

Pin	Assembly	Pin name	Notes	GPIO	Ball
24		SAI2_TXFS		GPIO4_IO24	SOC.AJ17
25		SAI2_TXC		GPIO4_IO25	SOC.AH15
26		SAI2_TXD0		GPIO4_IO26	SOC.AH16
27		GND	Digital Ground		GND
28		GND	Digital Ground		GND
29		GPIO1_IO15		GPIO1_IO15	SOC.B5
30		ENET_MDIO	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled	GPIO1_IO17	SOC.AH29
31	no QSPI and no SDEX	NC	Without "QSPI" or “SDEX” configuration this pin is Not Connected		NC_QSPI_SDEX
31	QSPI	NAND_DATA01	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	GPIO3_IO07	SOC.L25
31	SDEX	CONN_SD1_DATA1	Available in SOM with “SDEX” configuration. Pin referenced to 1.8V	GPIO2_IO03	SOC.Y28
32		VCC_SOM	SOM Power		VCC_SOM
33	no QSPI and no SDEX	NC	Without "QSPI" or “SDEX” configuration this pin is Not Connected		NC_QSPI_SDEX
33	QSPI	NAND_DATA02	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	GPIO3_IO08	SOC.L24
33	SDEX	CONN_SD1_DATA2	Available in SOM with “SDEX” configuration. Pin referenced to 1.8V	GPIO2_IO04	SOC.V29
34		VCC_SOM	SOM Power		VCC_SOM
35	no QSPI and no SDEX	NC	Without "QSPI" or “SDEX” configuration this pin is Not Connected		NC_QSPI_SDEX
35	QSPI	NAND_DATA03	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	GPIO3_IO09	SOC.N24
35	SDEX	CONN_SD1_DATA3	Available in SOM with “SDEX” configuration. Pin referenced to 1.8V	GPIO2_IO05	SOC.V28
36	no EC	VDD_ENET0_1P8_3P3_IN	ENET_QOS pins group power IN		VDD_ENET0_1P8_3P3_IN
36	EC	NC	With "EC" configuration this pin in Not Connected		NC
37		GND	Digital Ground		GND
38		VDD_ENET1_1P8_3P3_IN	ENET1 pins group power IN		VDD_ENET1_1P8_3P3_IN
39		ECSPI2_SS0		GPIO5_IO13	SOC.AJ22
40	no SAI1	GPIO1_IO00		GPIO1_IO00	SOC.A7
40	SAI1	SAI1_MCLK	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO20	SOC.AE12
41		ECSPI2_MISO		GPIO5_IO12	SOC.AH20
42		BOOT_SEL	Controls internal OR external boot source; Internal signal pulled up to SOM_PER_3V3 using 10K resistor;		INT. LOGIC
43		ECSPI2_SCLK		GPIO5_IO10	SOC.AH21
44		UART3_RXD		GPIO5_IO26	SOC.AE6
45		ECSPI2_MOSI		GPIO5_IO11	SOC.AJ21
46		UART3_TXD		GPIO5_IO27	SOC.AJ4
47		GND	Digital Ground		GND

Pin	Assembly	Pin name	Notes	GPIO	Ball
48		SAI2_MCLK	Dual pin, exported also on pin 191 in no TP and WBE	GPIO4_IO27	SOC.AJ15
49		SOM_3V3_PER	SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw allowed.		SOM_3V3_PER
50		ECSPI1_MISO	Used internally with "WBD", Function can be released if BT Function disabled	GPIO5_IO08	SOC.AD20
51		ECSPI1_SS0	Used internally with "WBD", Function can be released if BT Function disabled	GPIO5_IO09	SOC.AE20
52		ECSPI1_MOSI	Used internally with "WBD", Function can be released if BT Function disabled	GPIO5_IO07	SOC.AC20
53		ECSPI1_SCLK	Used internally with "WBD", Function can be released if BT Function disabled	GPIO5_IO06	SOC.AF20
54		SAI1_RXD7	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO09	SOC.AH12
55		SAI1_TXD3	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO15	SOC.AD12
56		SAI1_TXD2	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO14	SOC.AH11
57		SAI1_TXC	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO11	SOC.AJ12
58	no EC	ENET_TXC	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	GPIO1_IO23	SOC.AE24
58	EC	NC	With "EC" configuration this pin in Not Connected		NC_EC
59		GND	Digital Ground		GND
60		SD2_CLK	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO13	SOC.AB29
61		SD2_DATA2	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO17	SOC.AA26
62		SD2_DATA0	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO15	SOC.AC28
63		SD2_DATA1	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO16	SOC.AC29
64		SD2_CMD	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO14	SOC.AB28
65		SD2_DATA3	Bank voltage set on SOM 1.8V/3.3V	GPIO2_IO18	SOC.AA25
66		GND	Digital Ground		GND
67		GND	Digital Ground		GND
68		SPDIF_TX		GPIO5_IO03	SOC.AE18
69		GPIO1_IO11		GPIO1_IO11	SOC.D8
70	no SAI1 and no WBRST	GPIO1_IO13		GPIO1_IO13	SOC.A6
70	SAI1 and no WBRST	SAI1_RXD0	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO02	SOC.AC10
70	WBRST	IND_RST_BT	Pin referenced to 1.8V		LBES5PL2xL.64
71		SAI1_RXD6	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO08	SOC.AH10
72	no SAI1	GPIO1_IO05		GPIO1_IO05	SOC.B4

Pin	Assembly	Pin name	Notes	GPIO	Ball
	and no WBRST				
72	SAI1 and no WBRST	SAI1_RXD2	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO04	SOC.AH9
72	WBRST	NC	With "WBRST " configuration this pin in Not Connected		NC_WBRST
73		SAI1_TXD0	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO12	SOC.AJ11
74		ENET_MDC	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled	GPIO1_IO16	SOC.AH28
75	no SAI1 and no COEX	GPIO1_IO01		GPIO1_IO01	SOC.E8
75	SAI and no COEX	SAI1_RXD3	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO05	SOC.AJ8
75	COEX	WCI-2_OUT	Pin referenced to 1.8V		LBES5PL2xL.70
76		GND	Digital Ground		GND
77	no SAI1 and no COEX	GPIO1_IO08		GPIO1_IO08	SOC.A8
77	SAI and no COEX	SAI1_TXD6	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO18	SOC.AC12
77	COEX	NC	With "COEX" configuration this pin in Not Connected		NC_COEX
78		GND	Digital Ground		GND
79		NAND_DQS	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	GPIO3_IO14	SOC.R26
80		GPIO1_IO14		GPIO1_IO14	SOC.A4
81		SAI1_RXD5	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO07	SOC.AE10
82	no SAI1 and no WBRST	GPIO1_IO07		GPIO1_IO07	SOC.F6
82	SAI1 and no WBRST	SAI1_RXFS	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO00	SOC.AJ9
82	WBRST	IND_RST_WL	Pin referenced to 1.8V		LBES5PL2xL.63
83		UART2_RXD	Used as debug UART on Variscite base board	GPIO5_IO24	SOC.AF6
84	no SDEX	NAND_DATA00	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" and “no SDEX” configuration Pin is routed directly from CPU @1.8v	GPIO3_IO06	SOC.R25
84	SDEX	CONN_SD1_DATA0	Available in SOM with “SDEX” configuration. Pin referenced to 1.8V	GPIO2_IO02	SOC.Y29
85		UART2_TXD	Used as debug UART on Variscite base board	GPIO5_IO25	SOC.AH4
86	no SAI1 and no COEX	GPIO1_IO06		GPIO1_IO06	SOC.A3

Pin	Assembly	Pin name	Notes	GPIO	Ball
86	SAI1 and no COEX	SAI1_RXC	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO01	SOC.AH8
86	COEX	NC	With "COEX" configuration this pin in Not Connected		NC_COEX
87		I2C3_SDA		GPIO5_IO19	SOC.AJ6
88		I2C3_SCL		GPIO5_IO18	SOC.AJ7
89		GND	Digital Ground		GND
90		I2C4_SDA		GPIO5_IO21	SOC.AD8
91		USB1_RX_N			SOC.B9
92		I2C4_SCL		GPIO5_IO20	SOC.AF8
93		USB1_RX_P			SOC.A9
94		USB1_ID	USB PHY ID pin, No GPIO function Pin referenced to 1.8V		SOC.B11
95		GND	Digital Ground		GND
96		SAI1_TXD5	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter	GPIO4_IO17	SOC.AH14
97		USB1_TX_P			SOC.A10
98		SYS_nRST_3V3	SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset. By default, cold reset is performed power cycling the PMIC rails. Can be programmed to perform warm reset instead.		PMIC.8
99		USB1_TX_N			SOC.B10
100		PCIE1_REF_CLK_N	Differential Pair Negative side		SOC.E16
101		GND	Digital Ground		GND
102		PCIE1_REF_CLK_P	Differential Pair Positive side		SOC.D16
103		VCC_SOM	SOM Power		VCC_SOM
104		USB2_VBUS	USB PHY power pin; 5V tolerant		SOC.D12
105		VCC_SOM	SOM Power		VCC_SOM
106		USB1_VBUS	USB PHY power pin; 5V tolerant		SOC.A11
107		VCC_SOM	SOM Power		VCC_SOM
108		USB2_D_N			SOC.E14
109		VCC_SOM	SOM Power		VCC_SOM
110		USB2_D_P			SOC.D14
111		VCC_SOM	SOM Power		VCC_SOM
112		GND	Digital Ground		GND
113		SAI1_TXD4	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO16	SOC.AH13
114		USB1_D_N	USB OTG capable		SOC.E10
115		UART4_RXD		GPIO5_IO28	SOC.AJ5
116		USB1_D_P	USB OTG capable		SOC.D10
117	no SAI1 and no COEX	GPIO1_IO03		GPIO1_IO03	SOC.D6
117	SAI1 and no COEX	SAI1_RXD1	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO03	SOC.AF10
117	COEX	WCI-2_SIN			LBES5PL2xL.69

Pin	Assembly	Pin name	Notes	GPIO	Ball
118		GND	Digital Ground		GND
119		MIPI_CSI1_D0_P			SOC.D18
120		SAI1_TXFS	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO10	SOC.AF12
121		MIPI_CSI1_D0_N			SOC.E18
122		SAI1_RXD4	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO06	SOC.AD10
123		MIPI_CSI1_D1_N			SOC.E20
124		UART1_TXD		GPIO5_IO23	SOC.AJ3
125		MIPI_CSI1_D1_P			SOC.D20
126		GND	Digital Ground		GND
127		MIPI_CSI1_D2_P			SOC.D24
128		PCIE1_TX_N			SOC.B15
129		MIPI_CSI1_D2_N			SOC.E24
130		PCIE1_TX_P			SOC.A15
131		MIPI_CSI1_D3_N			SOC.E26
132		GND	Digital Ground		GND
133		MIPI_CSI1_D3_P			SOC.D26
134		PCIE1_RX_P			SOC.A14
135		MIPI_CSI1_CLK_P			SOC.D22
136		PCIE1_RX_N			SOC.B14
137		MIPI_CSI1_CLK_N			SOC.E22
138		GND	Digital Ground		GND
139		GND	Digital Ground		GND
140		USB2_RX_P			SOC.A12
141		USB2_TX_N			SOC.B13
142		USB2_RX_N			SOC.B12
143		USB2_TX_P			SOC.A13
144		GND	Digital Ground		GND
145	no QSPI and no SDEX	EARC_N_HPD	Available in SOM without "QSPI" or "SDEX" configuration; Pin referenced to 1.8v		SOC.AH22
145	QSPI	NAND_ALE	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	GPIO3_IO00	SOC.N25
145	SDEX	CONN_SD1_CLK	Available in SOM with "SDEX" configuration. Pin referenced to 1.8V	GPIO2_IO00	SOC.W28
146	no CSI2	HDMI_TX1_P	Available in SOM without "CSI2" configuration		SOC.AH26
146	CSI2	MIPI_CSI2_D1_P	Available in SOM with "CSI2" configuration		SOC.A24
147	no QSPI and no SDEX	EARC_P_UTIL	Available in SOM without "QSPI" or "SDEX" configuration; Pin referenced to 1.8v		SOC.AJ23
147	QSPI	NAND_CE0_B	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	GPIO3_IO01	SOC.L26
147	SDEX	CONN_SD1_CMD	Available in SOM with "SDEX" configuration. Pin referenced to 1.8V	GPIO2_IO01	SOC.W29
148	no CSI2	HDMI_TX1_N	Available in SOM without "CSI2" configuration		SOC.AJ26

Pin	Assembly	Pin name	Notes	GPIO	Ball
148	CSI2	MIPI_CSI2_D1_N	Available in SOM with "CSI2" configuration		SOC.B24
149		GND	Digital Ground		GND
150	no CSI2	HDMI_TXC_N	Available in SOM without "CSI2" configuration		SOC.AJ24
150	CSI2	MIPI_CSI2_CLK_N	Available in SOM with "CSI2" configuration		SOC.B23
151	no CSI2	HDMI_TX2_P	Available in SOM without "CSI2" configuration		SOC.AH27
151	CSI2	MIPI_CSI2_D2_P	Available in SOM with "CSI2" configuration		SOC.A22
152	no CSI2	HDMI_TXC_P	Available in SOM without "CSI2" configuration		SOC.AH24
152	CSI2	MIPI_CSI2_CLK_P	Available in SOM with "CSI2" configuration		SOC.A23
153	no CSI2	HDMI_TX2_N	Available in SOM without "CSI2" configuration		SOC.AJ27
153	CSI2	MIPI_CSI2_D2_N	Available in SOM with "CSI2" configuration		SOC.B22
154	no CSI2	HDMI_HPD	Available in SOM without "CSI2" configuration	GPIO3_IO29	SOC.AE22
154	CSI2	MIPI_CSI2_D3_P	Available in SOM with "CSI2" configuration		SOC.A21
155	no CSI2	HDMI_TX0_P	Available in SOM without "CSI2" configuration		SOC.AH25
155	CSI2	MIPI_CSI2_D0_P	Available in SOM with "CSI2" configuration		SOC.A25
156	no CSI2	HDMI_CEC	Available in SOM without "CSI2" configuration	GPIO3_IO28	SOC.AD22
156	CSI2	MIPI_CSI2_D3_N	Available in SOM with "CSI2" configuration		SOC.B21
157	no CSI2	HDMI_TX0_N	Available in SOM without "CSI2" configuration		SOC.AJ25
157	CSI2	MIPI_CSI2_D0_N	Available in SOM with "CSI2" configuration		SOC.B25
158		GND	Digital Ground		GND
159		GND	Digital Ground		GND
160	no DSI	LVDS0_D1_N	Available in SOM without "DSI" configuration		SOC.F28
160	DSI	MIPI_DSI1_D1_N	Available in SOM with "DSI" configuration		SOC.B17
161	no DSI	LVDS0_D0_N	Available in SOM without "DSI" configuration		SOC.E28
161	DSI	MIPI_DSI1_D0_N	Available in SOM with "DSI" configuration		SOC.B16
162	no DSI	LVDS0_D1_P	Available in SOM without "DSI" configuration		SOC.E29
162	DSI	MIPI_DSI1_D1_P	Available in SOM with "DSI" configuration		SOC.A17
163	no DSI	LVDS0_D0_P	Available in SOM without "DSI" configuration		SOC.D29
163	DSI	MIPI_DSI1_D0_P	Available in SOM with "DSI" configuration		SOC.A16
164	no DSI	LVDS0_D2_N	Available in SOM without "DSI" configuration		SOC.H28
164	DSI	MIPI_DSI1_D2_N	Available in SOM with "DSI" configuration		SOC.B19
165	no DSI	LVDS0_D3_N	Available in SOM without "DSI" configuration		SOC.J28
165	DSI	MIPI_DSI1_D3_N	Available in SOM with "DSI" configuration		SOC.B20
166	no DSI	LVDS0_D2_P	Available in SOM without "DSI" configuration		SOC.G29

Pin	Assembly	Pin name	Notes	GPIO	Ball
166	DSI	MIPI_DSI1_D2_P	Available in SOM with "DSI" configuration		SOC.A19
167	no DSI	LVDS0_D3_P	Available in SOM without "DSI" configuration		SOC.H29
167	DSI	MIPI_DSI1_D3_P	Available in SOM with "DSI" configuration		SOC.A20
168	no DSI	LVDS0_CLK_N	Available in SOM without "DSI" configuration		SOC.G28
168	DSI	MIPI_DSI1_CLK_N	Available in SOM with "DSI" configuration		SOC.B18
169		GND	Digital Ground		GND
170	no DSI	LVDS0_CLK_P	Available in SOM without "DSI" configuration		SOC.F29
170	DSI	MIPI_DSI1_CLK_P	Available in SOM with "DSI" configuration		SOC.A18
171		UART4_TXD		GPIO5_IO29	SOC.AH5
172		GND	Digital Ground		GND
173	no SAI1 and no WBRST	GPIO1_IO09		GPIO1_IO09	SOC.B8
173	SAI1 and no WBRST	SAI1_TXD7	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO19	SOC.AJ13
173	WBRST	IND_RST_15.4	Pin referenced to 1.8V		LBES5PL2xL.38
174		HDMI_DDC_SCL	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	GPIO3_IO26	SOC.AC22
175		UART1_RXD		GPIO5_IO22	SOC.AD6
176		HDMI_DDC_SDA	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	GPIO3_IO27	SOC.AF22
177		SAI1_TXD1	Referenced to pin 38 supply (1.8V/3.3V)	GPIO4_IO13	SOC.AJ10
178		GND	Digital Ground		GND
179		GND	Digital Ground		GND
180		LVDS1_CLK_N			SOC.B28
181		LVDS1_D3_P			SOC.C29
182		LVDS1_CLK_P			SOC.A28
183		LVDS1_D3_N			SOC.D28
184		LVDS1_D0_N			SOC.B26
185		GND	Digital Ground		GND
186		LVDS1_D0_P			SOC.A26
187	no TP	I2C1_SDA	Available in SOM without TP	GPIO5_IO15	SOC.AH7
187	TP	TS_X-	Signal source is Resistive Touch controller		TSC2046.8
188		LVDS1_D1_N			SOC.B27
189	no TP	I2C1_SCL	Available in SOM without TP	GPIO5_IO14	SOC.AC8
189	TP	TS_X+	Signal source is Resistive Touch controller		TSC2046.6
190		LVDS1_D1_P			SOC.A27
191	no TP and no WBE	I2C2_SDA	Available in SOM without TP and without WBE	GPIO5_IO17	SOC.AE8
191	no TP and WBE	SAI2_MCLK	Available in SOM without TP and with WBE; Dual pin, exported also on pin 48	GPIO4_IO27	SOC.AJ15
191	TP	TS_Y+	Signal source is Resistive Touch controller		TSC2046.7

Pin	Assembly	Pin name	Notes	GPIO	Ball
192		LVDS1_D2_N			SOC.C28
193	no TP	I2C2_SCL	Available in SOM without TP	GPIO5_IO16	SOC.AH6
193	TP	TS_Y-	Signal source is Resistive Touch controller		TSC2046.9
194		LVDS1_D2_P			SOC.B29
195		AGND	Audio Ground		AGND
196	no AC	SAI3_RXFS	Available in SOM without "AC" configuration	GPIO4_IO28	SOC.AJ19
196	AC	HPOUTFB	Signal source is Audio Codec		WM8904.14
197	no AC	SAI3_RXC	Available in SOM without "AC" configuration	GPIO4_IO29	SOC.AJ18
197	AC	LINEIN1_LP	Signal source is Audio Codec		WM8904.26
198	no AC	SAI3_RXD	Available in SOM without "AC" configuration	GPIO4_IO30	SOC.AF18
198	AC	HPLOUT	Signal source is Audio Codec		WM8904.13
199	no AC	SAI3_TXFS	Available in SOM without "AC" configuration	GPIO4_IO31	SOC.AC16
199	AC	LINEIN1_RP	Signal source is Audio Codec		WM8904.24
200	no AC	SAI3_TXC	Available in SOM without "AC" configuration	GPIO5_IO00	SOC.AH19
200	AC	HPROUT	Signal source is Audio Codec		WM8904.15

7.5 VAR-SOM-MX8M-PLUS Connector Pin Mux

Table 3: VAR-SOM-MX8M-PLUS PINMUX

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
1	no EC	SOC.AF24	ENET_QOS_RGMII_TX_CTL		SAI6_MCLK	SPDIF1_OUT		GPIO1_IO22	USDHC3_DATA0
3	no EC	SOC.AD24	ENET_QOS_RGMII_TD3		SAI6_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO18	USDHC3_DATA6
4	no EC	SOC.AG29	ENET_QOS_RGMII_RD0		SAI7_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO26	USDHC3_DATA4
5	no EC	SOC.AF26	ENET_QOS_RGMII_TD2	ENET_QOS_INPUT=ENET_ QOS_TX_CLK OUTPUT=CCM_ENET _QOS_REF_CLK_ROOT	SAI6_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO19	USDHC3_DATA7
6	no EC	SOC.AG28	ENET_QOS_RGMII_RD1		SAI7_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO27	USDHC3_RESET_B
9	no EC	SOC.AE26	ENET_QOS_RGMII_TD1		SAI6_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO20	USDHC3_CD_B
10	no EC	SOC.AF29	ENET_QOS_RGMII_RD2		SAI7_RX_BCLK	PDM_CLK		GPIO1_IO28	USDHC3_CLK
11	no EC	SOC.AC25	ENET_QOS_RGMII_TD0		SAI6_RX_BCLK	PDM_CLK		GPIO1_IO21	USDHC3_WP
12	no EC	SOC.AF28	ENET_QOS_RGMII_RD3		SAI7_MCLK	SPDIF1_IN		GPIO1_IO29	USDHC3_CMD
15	no EC	SOC.AE28	ENET_QOS_RGMII_RX_CTL		SAI7_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO24	USDHC3_DATA2
16	no EC	SOC.AE29	ENET_QOS_RGMII_RXC	ENET_QOS_RX_ER	SAI7_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO25	USDHC3_DATA3
17		SOC.AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO05	
18	no AC	SOC.AH18	SAI3_TX_DATA0	SAI2_TX_DATA3	SAI5_RX_DATA3	GPT1_CAPTURE2	SPDIF1_EXT_CLK	GPIO5_IO01	SRC_BOOT_MODE5
20	no AC	SOC.AJ20	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO02	SPDIF1_IN
21		SOC.AJ14	SAI2_RX_DATA0	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_ OUT	SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO23	PDM_BIT_STREAM3
22		SOC.AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1
23		SOC.AH17	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM2
24		SOC.AJ17	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_ OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2
25		SOC.AH15	SAI2_TX_BCLK	SAI5_TX_DATA2		FLEXCAN1_RX		GPIO4_IO25	PDM_BIT_STREAM1
26		SOC.AH16	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_ IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_ AUX_IN	GPIO4_IO26	SRC_BOOT_MODE4
29		SOC.B5	GPIO1_IO15	USB2_OTG_OC			USDHC3_WP	PWM4_OUT	CCM_CLKO2
30		SOC.AH29	ENET_QOS_MDIO		SAI6_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO17	USDHC3_DATA5
31	QSPI	SOC.L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_0	UART4_TX	GPIO3_IO07	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
31	SDEX	SOC.Y28	USDHC1_DATA1	ENET1_RGMII_TD0		I2C6_SDA	UART1_CTS_B	GPIO2_IO03	
33	QSPI	SOC.L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B	I2C4_SDA	GPIO3_IO08	
33	SDEX	SOC.V29	USDHC1_DATA2	ENET1_RGMII_RD0		I2C4_SCL	UART2_TX	GPIO2_IO04	
35	QSPI	SOC.N24	NAND_DATA03	QSPI_A_DATA3	USDHC3_WP	UART4_RTS_B	ISP_FL_TRIG_1	GPIO3_IO09	
35	SDEX	SOC.V28	USDHC1_DATA3	ENET1_RGMII_RD1		I2C4_SDA	UART2_RX	GPIO2_IO05	
39		SOC.AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13	
40	no SAI1	SOC.A7	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		CCM_REF_CLK_32K	CCM_EXT_CLK1
40	SAI1	SOC.AE12	SAI1_MCLK		SAI1_TX_BCLK		ENET1_INPUT=ENET1_TX_ CLK OUTPUT=CCM_ENET_REF_ CLK_ROOT	GPIO4_IO20	
41		SOC.AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	GPIO5_IO12	
43		SOC.AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10	
44		SOC.AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	FLEXCAN2_TX	GPIO5_IO26	
45		SOC.AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11	
46		SOC.AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	FLEXCAN2_RX	GPIO5_IO27	
48		SOC.AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_ IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_ AUX_IN	GPIO4_IO27	SAI3_MCLK
50		SOC.AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RX_DATA0		GPIO5_IO08	
51		SOC.AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC		GPIO5_IO09	
52		SOC.AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RX_BCLK		GPIO5_IO07	
53		SOC.AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RX_SYNC		GPIO5_IO06	
54		SOC.AH12	SAI1_RX_DATA7	SAI6_MCLK	SAI1_TX_SYNC	SAI1_TX_DATA4	ENET1_RGMII_RD3	GPIO4_IO09	
55		SOC.AD12	SAI1_TX_DATA3				ENET1_RGMII_TD3	GPIO4_IO15	
56		SOC.AH11	SAI1_TX_DATA2				ENET1_RGMII_TD2	GPIO4_IO14	
57		SOC.AJ12	SAI1_TX_BCLK				ENET1_RGMII_RXC	GPIO4_IO11	
58	no EC	SOC.AE24	ENET_QOS_RGMII_TXC	ENET_QOS_TX_ER	SAI7_TX_DATA0			GPIO1_IO23	USDHC3_DATA1
60		SOC.AB29	USDHC2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13	
61		SOC.AA26	USDHC2_DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO17	
62		SOC.AC28	USDHC2_DATA0		I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO15	
63		SOC.AC29	USDHC2_DATA1		I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO16	
64		SOC.AB28	USDHC2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14	
65		SOC.AA25	USDHC2_DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO18	SRC_EARLY_RESET

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
68		SOC.AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO03	
69		SOC.D8	GPIO1_IO11	USB2_OTG_ID	PWM2_OUT		USDHC3_VSELECT	CCM_PMIC_READY	
70	no SAI1 and no WBRST	SOC.A6	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	
70	SAI1 and no WBRST	SOC.AC10	SAI1_RX_DATA0		SAI1_TX_DATA1	PDM_BIT_STREAM0	ENET1_1588_EVENT1_IN	GPIO4_IO02	
71		SOC.AH10	SAI1_RX_DATA6	SAI6_TX_SYNC	SAI6_RX_SYNC		ENET1_RGMII_RD2	GPIO4_IO08	
72	no SAI1 and no WBRST	SOC.B4	GPIO1_IO05	M7_NMI		ISP_FL_TRIG_1		CCM_PMIC_READY	
72	SAI1 and no WBRST	SOC.AH9	SAI1_RX_DATA2			PDM_BIT_STREAM2	ENET1_MDC	GPIO4_IO04	
73		SOC.AJ11	SAI1_TX_DATA0				ENET1_RGMII_TD0	GPIO4_IO12	
74		SOC.AH28	ENET_QOS_MDC		SAI6_TX_DATA0			GPIO1_IO16	USDHC3_STROBE
75	no SAI1 and no COEX	SOC.E8	GPIO1_IO01	PWM1_OUT		ISP_SHUTTER_TRIG_0		CCM_REF_CLK_24M	CCM_EXT_CLK2
75	SAI and no COEX	SOC.AJ8	SAI1_RX_DATA3			PDM_BIT_STREAM3	ENET1_MDIO	GPIO4_IO05	
77	no SAI1 and no COEX	SOC.A8	GPIO1_IO08	ENET_QOS_1588_EVENT0_IN	PWM1_OUT	ISP_PRELIGHT_TRIG_1	ENET_QOS_1588_EVENT0_AUX_IN	USDHC2_RESET_B	
77	SAI and no COEX	SOC.AC12	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		ENET1_RX_ER	GPIO4_IO18	
79		SOC.R26	NAND_DQS	QSPI_A_DQS	SAI3_MCLK	ISP_SHUTTER_OPEN_0	I2C3_SCL	GPIO3_IO14	
80		SOC.A4	GPIO1_IO14	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1
81		SOC.AE10	SAI1_RX_DATA5	SAI6_TX_DATA0	SAI6_RX_DATA0	SAI1_RX_SYNC	ENET1_RGMII_RD1	GPIO4_IO07	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
82	no SAI1 and no WBRST	SOC.F6	GPIO1_IO07	ENET_QOS_MDIO		ISP_FLASH_TRIG_1		USDHC1_WP	CCM_EXT_CLK4
82	SAI1 and no WBRST	SOC.AJ9	SAI1_RX_SYNC				ENET1_1588_EVENT0_IN	GPIO4_IO00	
83		SOC.AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24	
84	no SDEX	SOC.R25	NAND_DATA00	QSPI_A_DATA0	SAI3_RX_DATA0	ISP_FLASH_TRIG_0	UART4_RX	GPIO3_IO06	
84	SDEX	SOC.Y29	USDHC1_DATA0	ENET1_RGMII_TD1		I2C6_SCL	UART1_RTS_B	GPIO2_IO02	
85		SOC.AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25	
86	no SAI1 and no COEX	SOC.A3	GPIO1_IO06	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		USDHC1_CD_B	CCM_EXT_CLK3
86	SAI1 and no COEX	SOC.AH8	SAI1_RX_BCLK			PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO01	
87		SOC.AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19	
88		SOC.AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18	
90		SOC.AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21	
91		SOC.B9	USB1_RX_N						
92		SOC.AF8	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20	
93		SOC.A9	USB1_RX_P						
94		SOC.B11	USB1_ID						
96		SOC.AH14	SAI1_TX_DATA5	SAI6_RX_DATA0	SAI6_TX_DATA0		ENET1_RGMII_TXC	GPIO4_IO17	
97		SOC.A10	USB1_TX_P						
99		SOC.B10	USB1_TX_N						
100		SOC.E16	PCIE_REF_PAD_CLK_N						
102		SOC.D16	PCIE_REF_PAD_CLK_P						
104		SOC.D12	USB2_VBUS						
106		SOC.A11	USB1_VBUS						
108		SOC.E14	USB2_D_N						
110		SOC.D14	USB2_D_P						
113		SOC.AH13	SAI1_TX_DATA4	SAI6_RX_BCLK	SAI6_TX_BCLK		ENET1_RGMII_TX_CTL	GPIO4_IO16	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
114		SOC.E10	USB1_D_N						
115		SOC.AJ5	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28	
116		SOC.D10	USB1_D_P						
117	no SAI1 and no COEX	SOC.D6	GPIO1_IO03	USDHC1_VSELECT		ISP_PRELIGHT_TRIG_0		SDMA1_EXT_EVENT0	
117	SAI1 and no COEX	SOC.AF10	SAI1_RX_DATA1			PDM_BIT_STREAM1	ENET1_1588_EVENT1_OUT	GPIO4_IO03	
119		SOC.D18	MIPI_CSI1_D0_P						
120		SOC.AF12	SAI1_TX_SYNC				ENET1_RGMII_RX_CTL	GPIO4_IO10	
121		SOC.E18	MIPI_CSI1_D0_N						
122		SOC.AD10	SAI1_RX_DATA4	SAI6_TX_BCLK	SAI6_RX_BCLK		ENET1_RGMII_RD0	GPIO4_IO06	
123		SOC.E20	MIPI_CSI1_D1_N						
124		SOC.AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23	
125		SOC.D20	MIPI_CSI1_D1_P						
127		SOC.D24	MIPI_CSI1_D2_P						
128		SOC.B15	PCIE_TXN_N						
129		SOC.E24	MIPI_CSI1_D2_N						
130		SOC.A15	PCIE_TXN_P						
131		SOC.E26	MIPI_CSI1_D3_N						
133		SOC.D26	MIPI_CSI1_D3_P						
134		SOC.A14	PCIE_RXN_P						
135		SOC.D22	MIPI_CSI1_CLK_P						
136		SOC.B14	PCIE_RXN_N						
137		SOC.E22	MIPI_CSI1_CLK_N						
140		SOC.A12	USB2_RX_P						
141		SOC.B13	USB2_TX_N						
142		SOC.B12	USB2_RX_N						
143		SOC.A13	USB2_TX_P						
145	no QSPI and no SDEX	SOC.AH22	EARC_N_HPD						
145	QSPI	SOC.N25	NAND_ALE	QSPI_A_SCLK	SAI3_TX_BCLK	ISP_FL_TRIG_0	UART3_RX	GPIO3_IO00	
145	SDEX	SOC.W28	USDHC1_CLK	ENET1_MDC		I2C5_SCL	UART1_TX	GPIO2_IO00	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
146	no CSI2	SOC.AH26	HDMI_TX1_P						
146	CSI2	SOC.A24	MIPI_CSI2_D1_P						
147	no QSPI and no SDEX	SOC.AJ23	EARC_P_UTIL						
147	QSPI	SOC.L26	NAND_CE0_B	QSPI_A_SS0_B	SAI3_TX_DATA0	ISP_SHUTTER_TRIG_0	UART3_TX	GPIO3_IO01	
147	SDEX	SOC.W29	USDHC1_CMD	ENET1_MDIO		I2C5_SDA	UART1_RX	GPIO2_IO01	
148	no CSI2	SOC.AJ26	HDMI_TX1_N						
148	CSI2	SOC.B24	MIPI_CSI2_D1_N						
150	no CSI2	SOC.AJ24	HDMI_TXC_N						
150	CSI2	SOC.B23	MIPI_CSI2_CLK_N						
151	no CSI2	SOC.AH27	HDMI_TX2_P						
151	CSI2	SOC.A22	MIPI_CSI2_D2_P						
152	no CSI2	SOC.AH24	HDMI_TXC_P						
152	CSI2	SOC.A23	MIPI_CSI2_CLK_P						
153	no CSI2	SOC.AJ27	HDMI_TX2_N						
153	CSI2	SOC.B22	MIPI_CSI2_D2_N						
154	no CSI2	SOC.AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	FLEXCAN2_RX	GPIO3_IO29	
154	CSI2	SOC.A21	MIPI_CSI2_D3_P						
155	no CSI2	SOC.AH25	HDMI_TX0_P						
155	CSI2	SOC.A25	MIPI_CSI2_D0_P						
156	no CSI2	SOC.AD22	HDMI_CEC			I2C6_SCL	FLEXCAN2_TX	GPIO3_IO28	
156	CSI2	SOC.B21	MIPI_CSI2_D3_N						
157	no CSI2	SOC.AJ25	HDMI_TX0_N						
157	CSI2	SOC.B25	MIPI_CSI2_D0_N						
160	no DSI	SOC.F28	LVDS0_D1_N						
160	DSI	SOC.B17	MIPI_DSI1_D1_N						
161	no DSI	SOC.E28	LVDS0_D0_N						
161	DSI	SOC.B16	MIPI_DSI1_D0_N						
162	no DSI	SOC.E29	LVDS0_D1_P						
162	DSI	SOC.A17	MIPI_DSI1_D1_P						
163	no DSI	SOC.D29	LVDS0_D0_P						
163	DSI	SOC.A16	MIPI_DSI1_D0_P						
164	no DSI	SOC.H28	LVDS0_D2_N						

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
164	DSI	SOC.B19	MIPI_DSI1_D2_N						
165	no DSI	SOC.J28	LVDS0_D3_N						
165	DSI	SOC.B20	MIPI_DSI1_D3_N						
166	no DSI	SOC.G29	LVDS0_D2_P						
166	DSI	SOC.A19	MIPI_DSI1_D2_P						
167	no DSI	SOC.H29	LVDS0_D3_P						
167	DSI	SOC.A20	MIPI_DSI1_D3_P						
168	no DSI	SOC.G28	LVDS0_CLK_N						
168	DSI	SOC.B18	MIPI_DSI1_CLK_N						
170	no DSI	SOC.F29	LVDS0_CLK_P						
170	DSI	SOC.A18	MIPI_DSI1_CLK_P						
171		SOC.AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29	
173	no SAI1 and no WBRST	SOC.B8	GPIO1_IO09	ENET_QOS_1588_EVENT0_ OUT	PWM2_OUT	ISP_SHUTTER_OPEN_1	USDHC3_RESET_B	SDMA2_EXT_EVENT0	
173	SAI1 and no WBRST	SOC.AJ13	SAI1_TX_DATA7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19	
174		SOC.AC22	HDMI_SCL			I2C5_SCL	FLEXCAN1_TX	GPIO3_IO26	
175		SOC.AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22	
176		SOC.AF22	HDMI_SDA			I2C5_SDA	FLEXCAN1_RX	GPIO3_IO27	
177		SOC.AJ10	SAI1_TX_DATA1				ENET1_RGMII_TD1	GPIO4_IO13	
180		SOC.B28	LVDS1_CLK_N						
181		SOC.C29	LVDS1_D3_P						
182		SOC.A28	LVDS1_CLK_P						
183		SOC.D28	LVDS1_D3_N						
184		SOC.B26	LVDS1_D0_N						
186		SOC.A26	LVDS1_D0_P						
187	no TP	SOC.AH7	I2C1_SDA	ENET_QOS_MDIO		ECSPI1_MOSI		GPIO5_IO15	
188		SOC.B27	LVDS1_D1_N						
189	no TP	SOC.AC8	I2C1_SCL	ENET_QOS_MDC		ECSPI1_SCLK		GPIO5_IO14	
190		SOC.A27	LVDS1_D1_P						

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
191	no TP and no WBE	SOC.AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_ OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17	
191	no TP and WBE	SOC.AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_ IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_ AUX_IN	GPIO4_IO27	SAI3_MCLK
192		SOC.C28	LVDS1_D2_N						
193	no TP	SOC.AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_ IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_ AUX_IN	GPIO5_IO16	
194		SOC.B29	LVDS1_D2_P						
196	no AC	SOC.AJ19	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI5_RX_SYNC	SAI3_RX_DATA1	SPDIF1_IN	GPIO4_IO28	PDM_BIT_STREAM0
197	no AC	SOC.AJ18	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK
198	no AC	SOC.AF18	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0		UART2_RTS_B	GPIO4_IO30	PDM_BIT_STREAM1
199	no AC	SOC.AC16	SAI3_TX_SYNC	SAI2_TX_DATA1	SAI5_RX_DATA1	SAI3_TX_DATA1	UART2_RX	GPIO4_IO31	PDM_BIT_STREAM3
200	no AC	SOC.AH19	SAI3_TX_BCLK	SAI2_TX_DATA2	SAI5_RX_DATA2	GPT1_CAPTURE1	UART2_TX	GPIO5_IO00	PDM_BIT_STREAM2

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe Clock, TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI (CSI and DSI), LVDS, HDMI	100 Ω Differential

8.2 Display Interfaces

the i.MX 8M Plus SoC has the following display support

- Three LCDIF Display Controllers:
  - One LCDIF drives MIPI DSI
  - One LCDIF drives LVDS Tx
  - One LCDIF drives HDMI Tx

Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.

The VAR-SOM-MX8M-PLUS supports all display interfaces HDMI, MIPI DSI and LVDS display available by the i.MX 8M Plus SoC

8.2.1 HDMI

The following features are supported:

HDMI 2.0a Tx supporting one display

- Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120,
- 3840 x 2160p30
- Pixel clock up to 297 MHz

Audio support

- 32 channel audio output support
- 1 S/PDIF audio eARC input support

8.2.1.1 HDMI Signals

Table 5: HDMI Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
156	no CSI2	HDMI_CEC	0	Available in SOM without "CSI2" configuration	SOC.AD22
154	no CSI2	HDMI_HPD	0	Available in SOM without "CSI2" configuration	SOC.AE22
154	no CSI2	HDMI_HPD_O	1	Available in SOM without "CSI2" configuration	SOC.AE22
174		HDMI_SCL	0	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AC22
176		HDMI_SDA	0	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AF22
157	no CSI2	HDMI_TX0_N	0	Differential Pair Negative side Available in SOM without "CSI2" configuration	SOC.AJ25
155	no CSI2	HDMI_TX0_P	0	Differential Pair Positive side Available in SOM without "CSI2" configuration	SOC.AH25
148	no CSI2	HDMI_TX1_N	0	Differential Pair Negative side Available in SOM without "CSI2" configuration	SOC.AJ26
146	no CSI2	HDMI_TX1_P	0	Differential Pair Positive side Available in SOM without "CSI2" configuration	SOC.AH26
153	no CSI2	HDMI_TX2_N	0	Differential Pair Negative side Available in SOM without "CSI2" configuration	SOC.AJ27
151	no CSI2	HDMI_TX2_P	0	Differential Pair Positive side Available in SOM without "CSI2" configuration	SOC.AH27
150	no CSI2	HDMI_TXC_N	0	Differential Pair Negative side Available in SOM without "CSI2" configuration	SOC.AJ24
152	no CSI2	HDMI_TXC_P	0	Differential Pair Positive side Available in SOM without "CSI2" configuration	SOC.AH24

Table 6: HDMI eARC Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
145	no QSPI and no SDEX	EARC_N_HPD	0	Differential Pair Negative side Available in SOM without "QSPI" configuration	SOC.AH22
147	no QSPI and no SDEX	EARC_P_UTIL	0	Differential Pair Positive side Available in SOM without "QSPI" configuration	SOC.AJ23

8.2.2 LVDS

The LVDS Display Bridge (LDB) connects the CPU internal LCDIF to External LVDS Display. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

The LVDS ports can be used as follows:

- Single channel (4 lanes) supports resolutions up to 720p60
- Dual asynchronous channels (8 data, 2 clocks). Supports resolutions up to 1920x1200p60 This is intended for a single panel with two interfaces, transferring across two channels (even pixel/odd pixel).

The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream. Splitting and reordering is required to match the LVDS Displays speed and channel requirements. Both VESA and JEIDA pixel mapping is supported.

8.2.2.1 LVDS0 Signals

Table 7: LVDS0 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
168	no DSI	LVDS0_CLK_N	0	Differential Pair Negative side Available in SOM without "DSI" configuration	SOC.G28
170	no DSI	LVDS0_CLK_P	0	Differential Pair Positive side Available in SOM without "DSI" configuration	SOC.F29
161	no DSI	LVDS0_D0_N	0	Differential Pair Negative side Available in SOM without "DSI" configuration	SOC.E28
163	no DSI	LVDS0_D0_P	0	Differential Pair Positive side Available in SOM without "DSI" configuration	SOC.D29
160	no DSI	LVDS0_D1_N	0	Differential Pair Negative side Available in SOM without "DSI" configuration	SOC.F28
162	no DSI	LVDS0_D1_P	0	Differential Pair Positive side Available in SOM without "DSI" configuration	SOC.E29
164	no DSI	LVDS0_D2_N	0	Differential Pair Negative side Available in SOM without "DSI" configuration	SOC.H28
166	no DSI	LVDS0_D2_P	0	Differential Pair Positive side Available in SOM without "DSI" configuration	SOC.G29
165	no DSI	LVDS0_D3_N	0	Differential Pair Negative side Available in SOM without "DSI" configuration	SOC.J28
167	no DSI	LVDS0_D3_P	0	Differential Pair Positive side Available in SOM without "DSI" configuration	SOC.H29

8.2.2.2 LVDS1 Signals

Table 8: LVDS1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
180		LVDS1_CLK_N	0	Differential Pair Negative side	SOC.B28
182		LVDS1_CLK_P	0	Differential Pair Positive side	SOC.A28
184		LVDS1_D0_N	0	Differential Pair Negative side	SOC.B26
186		LVDS1_D0_P	0	Differential Pair Positive side	SOC.A26
188		LVDS1_D1_N	0	Differential Pair Negative side	SOC.B27
190		LVDS1_D1_P	0	Differential Pair Positive side	SOC.A27
192		LVDS1_D2_N	0	Differential Pair Negative side	SOC.C28
194		LVDS1_D2_P	0	Differential Pair Positive side	SOC.B29
183		LVDS1_D3_N	0	Differential Pair Negative side	SOC.D28
181		LVDS1_D3_P	0	Differential Pair Positive side	SOC.C29

8.2.3 DSI

The i.MX 8M Plus incorporates the MIPI DSI Host Controller.

The key features of the MIPI DSI include:

- Compliant to MIPI-DSI standard v1.2
- Support up to 4 data lanes
- Maximum resolution limited to resolutions achievable with a 250MHz pixel clock and active pixel rate of 200Mpixel/s with 24-bit RGB. This includes resolutions such as:
  - 1080 p60
  - WUXGA (1920x1200) at 60 Hz
  - 1920x1440 at 60 Hz
  - UWHD (2560x1080) at 60 Hz
  - WQHD (2560x1440) can be supported by reduced blanking mode
- Support 80Mbps - 1.5Gbps data rate in high speed operation
- Support 10Mbps data rate in low power operation

Note: MIPI DSI is available only in SOMs with the “DSI” assembly option.
In “DSI” assembly option LVDS0 interface pins are not available.

8.2.3.1 DSI Signals

Table 9: MIPI DSI Signals

in#	Assy	Pin Function	Alt#	Notes	Ball
168	DSI	MIPI_DSI1_CLK_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.B18
170	DSI	MIPI_DSI1_CLK_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.A18
161	DSI	MIPI_DSI1_D0_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.B16
163	DSI	MIPI_DSI1_D0_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.A16
160	DSI	MIPI_DSI1_D1_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.B17
162	DSI	MIPI_DSI1_D1_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.A17
164	DSI	MIPI_DSI1_D2_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.B19
166	DSI	MIPI_DSI1_D2_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.A19
165	DSI	MIPI_DSI1_D3_N	0	Differential Pair Negative side Available in SOM with "DSI" configuration	SOC.B20
167	DSI	MIPI_DSI1_D3_P	0	Differential Pair Positive side Available in SOM with "DSI" configuration	SOC.A20

8.3 Camera Interface

8.3.1 MIPI CSI-2

The VAR-SOM-MX8M-PLUS consists of 2x MIPI CSI-2 Host Controller which implements the protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

- MIPI D-PHY specification V1.2 (Board Approved)
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature (Board Approved)
- Support primary and secondary Image format
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - All of User defined Byte-based Data packet
- Support up to 4 lanes of D-PHY operating up to a maximum bit rate of 1.5 Gbps
- Interfaces
  - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
  - AMBA3.0 APB Slave for Register configuration.
  - Image output data buswidth: 32 bits
- Image memory size of SRAM is 4KB
- Pixel clock can be gated when no ppi data is coming

Note: MIPI CSI-2 2nd interface is available only in SOMs with the “CSI2” assembly option. In “CSI2” assembly option HDMI interface pins are not available.

8.3.1.1 MIPI-CSI2 #1 Signals

Table 10: MIPI-CSI2 #1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
137		MIPI_CSI1_CLK_N	0	Differential Pair Negative side	SOC.E22
135		MIPI_CSI1_CLK_P	0	Differential Pair Positive side	SOC.D22
121		MIPI_CSI1_D0_N	0	Differential Pair Negative side	SOC.E18
119		MIPI_CSI1_D0_P	0	Differential Pair Positive side	SOC.D18
123		MIPI_CSI1_D1_N	0	Differential Pair Negative side	SOC.E20
125		MIPI_CSI1_D1_P	0	Differential Pair Positive side	SOC.D20
129		MIPI_CSI1_D2_N	0	Differential Pair Negative side	SOC.E24
127		MIPI_CSI1_D2_P	0	Differential Pair Positive side	SOC.D24
131		MIPI_CSI1_D3_N	0	Differential Pair Negative side	SOC.E26
133		MIPI_CSI1_D3_P	0	Differential Pair Positive side	SOC.D26

8.3.1.2 MIPI-CSI2 #2 Signals

Table 11: MIPI-CSI2 #2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
150	CSI2	MIPI_CSI2_CLK_N	0	Differential Pair Negative side Available in SOM with "CSI2" configuration	SOC.B23
152	CSI2	MIPI_CSI2_CLK_P	0	Differential Pair Positive side Available in SOM with "CSI2" configuration	SOC.A23
157	CSI2	MIPI_CSI2_D0_N	0	Differential Pair Negative side Available in SOM with "CSI2" configuration	SOC.B25
155	CSI2	MIPI_CSI2_D0_P	0	Differential Pair Positive side Available in SOM with "CSI2" configuration	SOC.A25
148	CSI2	MIPI_CSI2_D1_N	0	Differential Pair Negative side Available in SOM with "CSI2" configuration	SOC.B24
146	CSI2	MIPI_CSI2_D1_P	0	Differential Pair Positive side Available in SOM with "CSI2" configuration	SOC.A24
153	CSI2	MIPI_CSI2_D2_N	0	Differential Pair Negative side Available in SOM with "CSI2" configuration	SOC.B22
151	CSI2	MIPI_CSI2_D2_P	0	Differential Pair Positive side Available in SOM with "CSI2" configuration	SOC.A22
156	CSI2	MIPI_CSI2_D3_N	0	Differential Pair Negative side Available in SOM with "CSI2" configuration	SOC.B21
154	CSI2	MIPI_CSI2_D3_P	0	Differential Pair Positive side Available in SOM with "CSI2" configuration	SOC.A21

8.3.2 ISP

The Image Signal Processors (ISP) receive an image from the camera sensor and converts it from raw Bayer to YUV so it can be processed by the chip. The ISP also provides additional processing to improve the image quality. Supported image quality processes include:

- HDR to retain image details in high contrast scenes
- Dewarp to correct the image geometry caused by lens distortion (e.g. fisheye lens)
- Image enhancements (e.g. AWB, Denoise, AE, etc)

There are two instances of ISP on the chip and each is connected to separate instances of MIPI CSI. Both ISP instances support YCbCr420, YCbCR422, RAW8, RAW10, and RAW12 output pixel formats.

8.3.2.1 High-Dynamic Range (HDR)

The ISP supports the following HDR generation for high-quality on-the-fly dynamic range compression (DRC):

- Native HDR Sensor with compand output (max 14 bit compressed input)
- Digital Overlap High-Dynamic Range Sensor (DOL-HDR), staggered HDR For Native HDR sensors, the multi-exposure stitching is done internally and has line buffers.

Table 12: ISP0 & ISP1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
40	no SAI1	ISP_FL_TRIG_0	3		SOC.A7
145	QSPI	ISP_FL_TRIG_0	3	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N25
35	QSPI	ISP_FL_TRIG_1	4	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N24
72	no SAI1 and no WBRST	ISP_FL_TRIG_1	3		SOC.B4
84	no SDEX	ISP_FLASH_TRIG_0	3	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R25
82	no SAI1 and no WBRST	ISP_FLASH_TRIG_1	3		SOC.F6
31	QSPI	ISP_PRELIGHT_TRIG_0	3	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L25
117	no SAI1 and no COEX	ISP_PRELIGHT_TRIG_0	3		SOC.D6
77	no SAI1 and no COEX	ISP_PRELIGHT_TRIG_1	3		SOC.A8
79		ISP_SHUTTER_OPEN_0	3	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R26
173	no SAI1 and no WBRST	ISP_SHUTTER_OPEN_1	3		SOC.B8
75	no SAI1 and no COEX	ISP_SHUTTER_TRIG_0	3		SOC.E8
147	QSPI	ISP_SHUTTER_TRIG_0	3	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L26
86	no SAI1 and no COEX	ISP_SHUTTER_TRIG_1	3		SOC.A3

8.4 Ethernet Interface

The iMX 8M Plus implements Two Ethernet controllers both capable of simultaneous operation.

ENET_QOS (Ethernet Quality of Service) - Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588

ENET1 - Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

8.4.1 ENET_QOS (Ethernet Quality of Service)

The SOM can be ordered in one of the following configurations:

- **"EC" configuration** – The VAR-SOM-MX8M-PLUS includes an on SOM a Gigabit PHY (MaxLinear MxL86110) connected to ENET_QOS RGMII interface signals. External connector and magnetics should be implemented on carrier board to complete the interface to the media.

- **"no EC" configuration** - The VAR-SOM-MX8M-PLUS exposes the ENET_QOS RGMII/RMII interface signals to the SO-DIMM connector and ENET_QOS pins are referenced to SOM pin 36 VDD_ENET0_1P8_3P3_IN.
  Reference voltage should be supplied to SOM pin 36:
  For RMII – 1.8V/3.3, For RGMII - 1.8V.

8.4.1.1 Ethernet PHY

The on SOM MaxLinear MxL86110x Gigabit PHY in conjunction with external magnetics on carrier board complete the interface to the media.
PHY LINK LEDs 10/100 and 1000 combined on SOM to one signal 10/100/1000.

The Following External Gigabit magnetics are required to complete the Ethernet PHY interface to the media.

Table 13: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

Table 14: Ethernet PHY Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
15	EC	ETH0_LED_ACT		Signal source is Ethernet PHY Ethernet PHY Activity LED, active low	MxL86110x.32
16	EC	ETH0_LED_LINK_10_100_1000		Signal source is Ethernet PHY Ethernet PHY Link LED, active low	MxL86110x.33
5	EC	ETH0_MDI_A_M		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.2
3	EC	ETH0_MDI_A_P		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.1
11	EC	ETH0_MDI_B_M		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.5
9		ETH0_MDI_B_P		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.4
6	EC	ETH0_MDI_C_M		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.7
4	EC	ETH0_MDI_C_P		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.6
12	EC	ETH0_MDI_D_M		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.10
10	EC	ETH0_MDI_D_P		Differential Pair Positive side Signal source is Ethernet PHY	MxL86110x.9
1	EC	NC		With "EC" configuration this pin in Not Connected	NC_EC
58	EC	NC		With "EC" configuration this pin in Not Connected	NC_EC
36	EC	NC		With "EC" configuration this pin in Not Connected	NC_EC

Table 155: MxL86110x Ethernet PHY LED Behavior

Symbol	10M link	10M active	100M link	100M active	1000M link	1000M active
LED_10_100_1000	ON	ON	ON	ON	ON	ON
LED_ACT	OFF	BLINK	OFF	BLINK	OFF	BLINK
ON = active; OFF = inactive						

8.4.1.2 ENET_QOS Signals

Table 166: ENET_QOS Supply voltage input Signal

Pin#	Assy	Pin Function	Alt#	Notes	Ball
36	no EC	VDD_ENET0_1P8_3P3_IN		ENET_QOS pins group power IN "EC" configuration: * Not Connected No "EC" configuration: NVCC_ENET 1.8V/3.3V supply voltage input. The following SOM pins are referenced to this voltage: 1,3,4,5,6,9,10,11,12,15,16,30,58,74. Must supply one option: * For RMII - connect to 1.8 or 3.3V. * For RGMII - connect to 1.8V * For other alternates - connect to 1.8V/3.3V	VDD_ENET0_1P8_3P3_IN

Table 177: ENET_QOS RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
77	no SAI1 and no COEX	ENET_QOS_1588_EVENT0_ AUX_IN	4		SOC.A8
77	no SAI1 and no COEX	ENET_QOS_1588_EVENT0_ IN	1		SOC.A8
173	no SAI1 and no WBRST	ENET_QOS_1588_EVENT0_ OUT	1		SOC.B8
193	no TP	ENET_QOS_1588_EVENT1_ AUX_IN	4	Available in SOM without TP	SOC.AH6
193	no TP	ENET_QOS_1588_EVENT1_ IN	1	Available in SOM without TP	SOC.AH6
191	no TP and no WBE	ENET_QOS_1588_EVENT1_ OUT	1	Available in SOM without TP	SOC.AE8
26		ENET_QOS_1588_EVENT2_ AUX_IN	4		SOC.AH16
26		ENET_QOS_1588_EVENT2_ IN	2		SOC.AH16
21		ENET_QOS_1588_EVENT2_ OUT	2		SOC.AJ14
48		ENET_QOS_1588_EVENT3_ AUX_IN	4	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
48		ENET_QOS_1588_EVENT3_ IN	2	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	ENET_QOS_1588_EVENT3_ AUX_IN	4	Dual pin, exported also on pin 48	SOC.AJ15

Pin#	Assy	Pin Function	Alt#	Notes	Ball
191	no TP and WBE	ENET_QOS_1588_EVENT3_ IN	2	Dual pin, exported also on pin 48	SOC.AJ15
24		ENET_QOS_1588_EVENT3_ OUT	2		SOC.AJ17
5	no EC	ENET_QOS_INPUT=ENET_ QOS_TX_CLK OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT	1	Referenced to pin 36 supply (1.8V/3.3V); RMII clock - can be used in 2 schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.	SOC.AF26
86	no SAI1 and no COEX	ENET_QOS_MDC	1		SOC.A3
74		ENET_QOS_MDC	0	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH28
30		ENET_QOS_MDIO	0	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH29
187	no TP	ENET_QOS_MDIO	1	Available in SOM without TP	SOC.AH7
82	no SAI1 and no WBRST	ENET_QOS_MDIO	1		SOC.F6
4	no EC	ENET_QOS_RGMII_RD0	0	Referenced to pin 36 supply (1.8V/3.3V); RMII/RGMI Data in	SOC.AG29
6	no EC	ENET_QOS_RGMII_RD1	0	Referenced to pin 36 supply (1.8V/3.3V); RMII/RGMI Data in	SOC.AG28
10	no EC	ENET_QOS_RGMII_RD2	0	Referenced to pin 36 supply (1.8V/3.3V); RGMII Data in;	SOC.AF29
12	no EC	ENET_QOS_RGMII_RD3	0	Referenced to pin 36 supply (1.8V/3.3V); RGMII Data in	SOC.AF28
15	no EC	ENET_QOS_RGMII_RX_CTL	0	Referenced to pin 36 supply (1.8V/3.3V); RMII - RX_EN (CRS_DV) Signal; RGMII - Receive Control signal	SOC.AE28
16	no EC	ENET_QOS_RGMII_RXC	0	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	SOC.AE29

Pin#	Assy	Pin Function	Alt#	Notes	Ball
11	no EC	ENET_QOS_RGMII_TD0	0	Referenced to pin 36 supply (1.8V/3.3V); RMII/RGMII Data out	SOC.AC25
9	no EC	ENET_QOS_RGMII_TD1	0	Referenced to pin 36 supply (1.8V/3.3V); RMII/RGMII Data out	SOC.AE26
5	no EC	ENET_QOS_RGMII_TD2	0	Referenced to pin 36 supply (1.8V/3.3V); RGMII Data out;	SOC.AF26
3	no EC	ENET_QOS_RGMII_TD3	0	Referenced to pin 36 supply (1.8V/3.3V); RGMII Data out	SOC.AD24
1	no EC	ENET_QOS_RGMII_TX_CTL	0	Referenced to pin 36 supply (1.8V/3.3V); RMII - TX_EN signal; RGMII - Transmit Control signal; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
58	no EC	ENET_QOS_RGMII_TXC	0	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AE24
16	no EC	ENET_QOS_RX_ER	1	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; RMII - RX_ER Signal	SOC.AE29
58	no EC	ENET_QOS_TX_ER	1	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; RMII - TX_ER signal; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AE24

8.4.2 ENET1

ENET1 RGMII/RMII interface signals are always exported through SO-DIMM connector.
Signals, in conjunction to MDIO signals exported from SO-DIMM connector, they can be used to interface an external Ethernet PHY.

ENET1 pins are referenced to SOM pin 38 VDD_ENET1_1P8_3P3_IN.
Reference voltage should be supplied to SOM pin 38.
For RMII – 1.8V/3.3 V
For RGMII - 1.8V

8.4.2.1 ENET1 Signals

Table 188: ENET1 Supply voltage input Signal

Pin#	Assy	Pin Function	Alt#	Notes	Ball
38		VDD_ENET1_1P8_3P3_IN		NVCC_SAI1_SAI5 supply voltage input. The following SOM pins are referenced to this voltage: 54,55,56,57,71,73,81,96,113,120,122,177 In "SAI1" configuration, also these pins are referenced to this voltage: 40,70,72,75,77,82,86,117,173 Must supply one option: * For RMII - connect to 1.8 or 3.3V. * For RGMII - connect to 1.8V * For other alternates - connect to 1.8V/3.3V	VDD_ENET1_1P8_3P3_IN

Table 199: ENET1 RMII/RGMII Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
82	SAI1 and no WBRST	ENET1_1588_EVENT0_IN	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ9
86	SAI1 and no COEX	ENET1_1588_EVENT0_OUT	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH8
70	SAI1 and no WBRST	ENET1_1588_EVENT1_IN	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC10
117	SAI1 and no COEX	ENET1_1588_EVENT1_OUT	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF10
40	SAI1	ENET1_INPUT=ENET1_TX_CLK OUTPUT=CCM_ENET_REF_CLK_ROOT	4	Referenced to pin 38 supply (1.8V/3.3V); RMII clock - can be used in 2 schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.	SOC.AE12
72	SAI1 and no WBRST	ENET1_MDC	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH9
145	SDEX	ENET1_MDC	1	Pin referenced to 1.8V	SOC.W28
75	SAI and no COEX	ENET1_MDIO	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ8
147	SDEX	ENET1_MDIO	1	Pin referenced to 1.8V	SOC.W29
122		ENET1_RGMII_RD0	4	Referenced to pin 38 supply (1.8V/3.3V); RMII/RGMI Data in	SOC.AD10
33	SDEX	ENET1_RGMII_RD0	1	Pin referenced to 1.8V	SOC.V29
81		ENET1_RGMII_RD1	4	Referenced to pin 38 supply (1.8V/3.3V); RMII/RGMI Data in	SOC.AE10
35	SDEX	ENET1_RGMII_RD1	1	Pin referenced to 1.8V	SOC.V28
71		ENET1_RGMII_RD2	4	Referenced to pin 38 supply (1.8V/3.3V); RGMII Data in;	SOC.AH10
54		ENET1_RGMII_RD3	4	Referenced to pin 38 supply (1.8V/3.3V); RGMII Data in	SOC.AH12
120		ENET1_RGMII_RX_CTL	4	Referenced to pin 38 supply (1.8V/3.3V); RMII - RX_EN (CRS_DV) Signal; RGMII Receive Control signal	SOC.AF12
57		ENET1_RGMII_RXC	4	Referenced to pin 38 supply (1.8V/3.3V) RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	SOC.AJ12
73		ENET1_RGMII_TD0	4	Referenced to pin 38 supply (1.8V/3.3V); RMII/RGMII Data out	SOC.AJ11
31	SDEX	ENET1_RGMII_TD0	1	Pin referenced to 1.8V	SOC.Y28
177		ENET1_RGMII_TD1	4	Referenced to pin 38 supply (1.8V/3.3V); RMII/RGMII Data out	SOC.AJ10

Pin#	Assy	Pin Function	Alt#	Notes	Ball
84	SDEX	ENET1_RGMII_TD1	1	Pin referenced to 1.8V	SOC.Y29
56		ENET1_RGMII_TD2	4	Referenced to pin 38 supply (1.8V/3.3V); RGMII Data out	SOC.AH11
55		ENET1_RGMII_TD3	4	Referenced to pin 38 supply (1.8V/3.3V); RGMII Data out	SOC.AD12
113		ENET1_RGMII_TX_CTL	4	Referenced to pin 38 supply (1.8V/3.3V); RMII - TX_EN signal; RGMII - Transmit Control signal	SOC.AH13
96		ENET1_RGMII_TXC	4	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples TD [3:0] and TX_CTL;	SOC.AH14
77	SAI and no COEX	ENET1_RX_ER	4	Referenced to pin 38 supply (1.8V/3.3V); RMII - RX_ER signal	SOC.AC12
173	SAI1 and no WBRST	ENET1_TX_ER	4	Referenced to pin 38 supply (1.8V/3.3V); RMII - TX_ER signal	SOC.AJ13

8.5 Wi-Fi & BT

The VAR-SOM-MX8M-PLUS contains a certified high-performance Wi-Fi, Bluetooth, 802.15.4 module:

- Wi-Fi® 802.11a/b/g/n/ac/ax
- Bluetooth® 5.3 BR/EDR/LE
- 802.15.4
- Modules have an antenna connection through a U. FL JACK connector
- Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SOM-MX8M-PLUS internal Wi-Fi and BT connectivity.

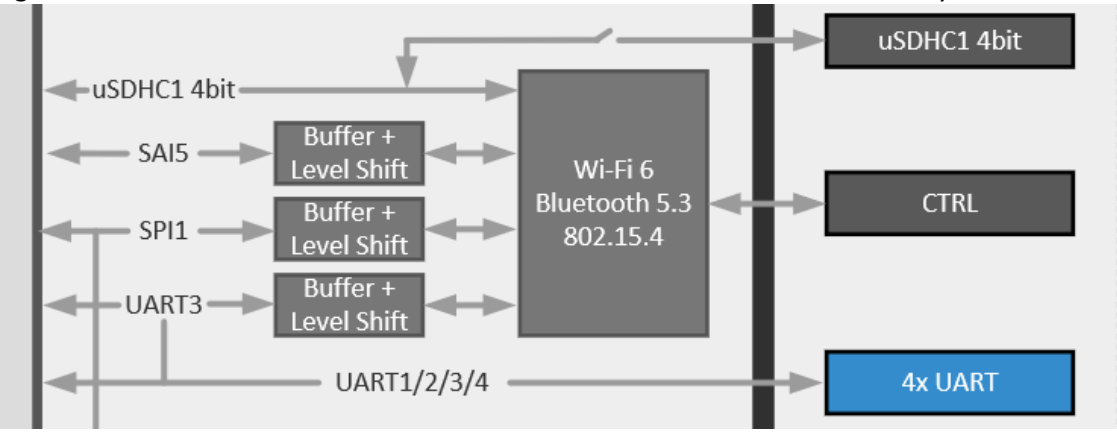


Figure 3: VAR-SOM-MX8M-PLUS Wi-Fi & BT Internal Connection

NOTE

BT, 802.15.14, BT UART buffer, BT PCM buffer are controlled using GPIO1_IO04.

- Logic “High” enables the BT, 802.15.14 and buffers.
- Logic “Low” disables them and releases the BT UART signals to be used via SOM connector.

8.5.1 Interface Implementation Options

8.5.1.1 Module Configuration with "WBD" Option

- System use**: Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffer (using GPIO1_IO04) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT buffer (using GPIO1_IO04) and BT function.

8.5.1.2 Module Configuration with "WBE" Option

- System use: **Wi-Fi and Bluetooth and 802.15.4**.
  - BT UART external interface pins should be left floating.
  - TP SPI pins can be used in SPI mode only
- System use: **Wi-Fi and no BT no 802.15.4**.
  - In this case, disable the BT and 802.15.4 module (using GPIO1_IO04)
  - BT UART and TP SPI interface pins can be used externally with any of the alternate functions.
- System use: **BT and 802.15.4 and no Wi-Fi.**
  - Disable Wi-Fi function.
  - Enable the BT and 802.15.4 module (using GPIO1_IO04).

8.5.1.3 Module Configuration without "WBD" or "WB" Option

- System use: **no Wi-Fi and no BT**.
  - BT UART interface accessible externally with any of its alternative functions.
  - uSDHC1 pins can be exported in SOM with special assembly "SDEX"
    SD1 is working at 1.8V levels

8.5.2 Bluetooth Interface Signals

Table 20: BT UART Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		UART3_CTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
51		UART3_RTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20
52		UART3_TX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AC20
53		UART3_RX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AF20

8.6 Ultra-Secured Digital Host Controller

The VAR-SOM-MX8M-PLUS exposes the uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards.
Key features of uSDHC2:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.1.
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

8.6.1 uSDHC1 Signals

uSDHC controller, uSDHC1, is used internally for the Wi-Fi SDIO interface on the SOM.
In case no Wi-Fi is assembled uSDHC1 pins can be exported in SOM with special assembly "SDEX".

Table 201: uSDHC1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
31	SDEX	USDHC1_DATA1	0	Pin referenced to 1.8V	SOC.Y28
33	SDEX	USDHC1_DATA2	0	Pin referenced to 1.8V	SOC.V29
35	SDEX	USDHC1_DATA3	0	Pin referenced to 1.8V	SOC.V28
84	SDEX	USDHC1_DATA0	0	Pin referenced to 1.8V	SOC.Y29
145	SDEX	USDHC1_CLK	0	Pin referenced to 1.8V	SOC.W28
147	SDEX	USDHC1_CMD	0	Pin referenced to 1.8V	SOC.W29

8.6.2 uSDHC2 Signals

For ***Card Detect function*** any GPIO can be used; For pinout compatibility with other SOMs of VAR-SOM pin2pin family, pin 80 GPIO1_IO14 is used.

Table 212: uSDHC2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
60		USDHC2_CLK	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
61		USDHC2_DATA2	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
62		USDHC2_DATA0	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
63		USDHC2_DATA1	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
64		USDHC2_CMD	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AB28
65		USDHC2_DATA3	0	Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
77	no SAI1	USDHC2_RESET_B	5		SOC.A8

8.6.3 uSDHC3 Signals

uSDHC controller, uSDHC3, is used internally for the eMMC interface on the SOM.

8.7 USB 3.0

The VAR-SOM-MX8M-PLUS consists Two USB controllers and PHYs that support USB 3.0 and USB 2.0.

Each USB 3.0 module includes the following features:

- Up to SDR104 rate
- Complies with USB specification rev 3.0 (xHCI compatible)
- Supports operation as a standalone USB host controller
  USB dual-role operation and can be configured as host or device
- Super-speed (5 Gbit/s), high-speed (480 Mbit/s), full-speed (12 Mbit/s), and lowspeed (1.5 Mbit/s) operations.
- Supports operation as a standalone single port USB
- Supports four programmable, bidirectional USB endpoints
- Supports system memory interface with -bit addressing capability

The USB 3.0 module operates in following modes.

- Host Mode: SS/HS/FS/LS
- Device Mode: SS/HS/FS

8.7.1 USB Port1 Interface Signals

Table 22: USB 3.0/2.0 Port 1 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
114		USB1_D_N	0	Differential Pair Negative side USB OTG capable	SOC.E10
116		USB1_D_P	0	Differential Pair Positive side USB OTG capable	SOC.D10
94		USB1_ID	0	USB PHY ID pin, No GPIO function USB OTG ID alternative signal location. "Low" means the SoC is Host role "High" means the SoC is Peripheral role. Pin referenced to 1.8V.	SOC.B11
91		USB1_RX_N	0	Differential Pair Negative side	SOC.B9
93		USB1_RX_P	0	Differential Pair Positive side	SOC.A9
99		USB1_TX_N	0	Differential Pair Negative side	SOC.B10
97		USB1_TX_P	0	Differential Pair Positive side	SOC.A10
106		USB1_VBUS	0	USB PHY power pin; 5V tolerant	SOC.A11

Note: Usage of native USB_ID in i.MX 8M -PLUS requires patches not included in NXP formal release. Pin referenced to 1.8V. For simple OTG implementation, use a CC Logic chip and connect to GPIO (see Symphony-Board implementation). USB1_ID can be left floating if not used.

8.7.2 USB Port2 Interface Signals

Table 23: USB 3.0/2.0 Port 2 Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
108		USB2_D_N	0	Differential Pair Negative side	SOC.E14
110		USB2_D_P	0	Differential Pair Positive side	SOC.D14
142		USB2_RX_N	0	Differential Pair Negative side	SOC.B12
140		USB2_RX_P	0	Differential Pair Positive side	SOC.A12
141		USB2_TX_N	0	Differential Pair Negative side	SOC.B13
143		USB2_TX_P	0	Differential Pair Positive side	SOC.A13
104		USB2_VBUS	0	USB PHY power pin; 5V tolerant	SOC.D12

8.7.3 USB OTG Interface Signals

The VAR-SOM-MX8M-PLUS exposes pins, which can be optionally used for additional functions.

Table 24: USB Port 1 & 2 OTG Interface signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
70	no SAI1	USB1_OTG_OC	1		SOC.A6
29		USB2_OTG_OC	1		SOC.B5
80		USB2_OTG_PWR	1		SOC.A4

8.8 PCIe

The VAR-SOM-MX8M-PLUS exposes a single PCI Express Gen 3.0 single lane interface.
The PCI Express port requires an external 100MHz PCIe compliant reference clock if the function is enabled.

The SOM exports the PCIE differential clock. These pins are bi-directional which can either be used to feed 100 MHz reference clock to the PHY from external clock source, or to output an internal generated 100 MHz reference clock to PCIE connector or PCIE device.
On the VAR-SOM-MX8M-PLUS carrier board, the Symphony-Board, a PCIE clock generator chip is used to feed high-quality clock to both the PHY and connecter/device.
The internal clock of the chip can be used instead of clock generator (requires SW modification). However, the internal clock exhibits larger jitter than that from PCIE clock generator and does not meet Gen 3.0 specification requirements.

The PCIe controller implements the following standards:

- PCI Express Base Specification, Revision 4.0, Version 0.7
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

The following list the key features of the Samsung PCIe PHY IP core used for PCI-Express (PCIe) applications:

- 2.5Gb/s, 5.0Gb/s, and 8.0Gb/s Serializer/De-serializer
- Serializes the 8b/10b encoded data for transmission for Gen1 and Gen2 operation, and 128b/130b encoded data for Gen3. De-serializes the received code groups
- PHY Interface for the PCI Express Architecture, Version 4.2 compliance
- Spread Spectrum Clocking in Transmitter and Receiver
- Separate Refclk Independent SSC (SRIS) Architecture
- Continuous-Time Linear Equalizer and 5-tap adaptive Decision-Feedback Equalizer

8.8.1 PCIE Signals

Table 25: PCIE Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
100		PCIE_REF_PAD_CLK_N	0	Differential Pair Negative side Differential Pair Negative side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector	SOC.E16
102		PCIE_REF_PAD_CLK_P	0	Differential Pair Positive side Differential Pair Positive side PCIE compliant 100MHz reference clock; Terminate with 49.9 Ohm close to the connector	SOC.D16
136		PCIE_RXN_N	0	Differential Pair Negative side	SOC.B14
134		PCIE_RXN_P	0	Differential Pair Positive side	SOC.A14
128		PCIE_TXN_N	0	Differential Pair Negative side	SOC.B15
130		PCIE_TXN_P	0	Differential Pair Positive side	SOC.A15

8.8.2 PCIE Side band signals

Table 26: PCIE Side band Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
92		PCIE1_CLKREQ_B	2		SOC.AF8
115		PCIE1_CLKREQ_B	2		SOC.AJ5

8.9 Audio

The VAR-SOM-MX8M-PLUS features the following audio interfaces:

- WM8904CGEFL Audio codec interfaces:
  - Analog outputs & inputs: stereo line-in & Stereo HP out.
  - Digital microphone input
- Five external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces:
  - SAI-1 supports to up to 16-channels TX (8 lanes) and 16-channels RX (8 lanes) at 768KHz/32-bit
  - SAI-2/5 supports to up to 8-channels TX (4 lanes) and 8-channels RX (4 lanes) at 768KHz/32-bit
  - SAI-3 supports up to 4-channels TX (2 lanes) and 4-channels RX (2 lanes) at 768KHz/32-bit
  - SAI-6 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 768KHz/32-bit when multiplexed on SAI1, or up to 384kHz/32-bit when multiplexed on Ethernet primary pins
  - SAI-7 supports to up to 2-channels TX (1 lanes) and 2-channels RX (1 lanes) at 384KHz/32-bit
- PDM supporting up to 8-channels (4 lanes)
- S/PDIF Input and Output, including a new Raw Capture input mode
- Hifi4 Audio DSP, operating up to 800 MHz

Analog audio signals are part of the SOM WM8904 audio codec, available with **"AC" Configuration** only. The codec interfaces the SoC via SAI3 lines, when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.

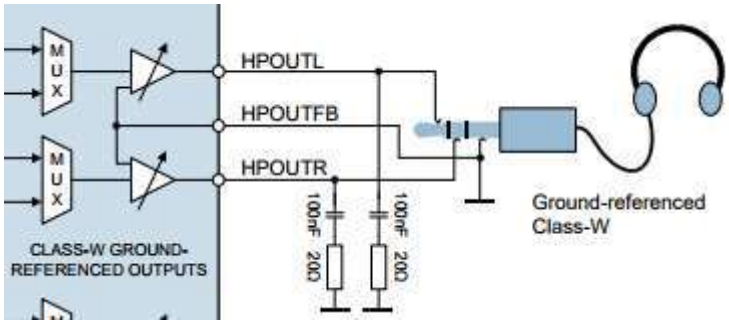


Figure 4: WM8904 Headphone connectivity

8.9.1 WM8904CGEFL Audio Codec

8.9.1.1 Audio Codec Signals

Table 27: Analog audio Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
195		AGND		Audio Ground	AGND
18	AC	DMIC_CLK		Signal source is Audio Codec Digital microphone clock output	WM8904.1
20	AC	DMIC_DATA		Signal source is Audio Codec Digital microphone data input; Divided internally by 475 Ohm resistors to match Codec input levels	WM8904.27
198	AC	HPLOUT		Signal source is Audio Codec Left headphone output (line or headphone output)	WM8904.13
196	AC	HPOUTFB		Signal source is Audio Codec Headphone output ground loop noise rejection feedback	WM8904.14
200	AC	HPROUT		Signal source is Audio Codec Right headphone output (line or headphone output)	WM8904.15
197	AC	LINEIN1_LP		Signal source is Audio Codec Left channel input	WM8904.26
199	AC	LINEIN1_RP		Signal source is Audio Codec Right channel input	WM8904.24

8.9.2 Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

8.9.2.1 SAI1 Signals

Table 28: Serial Audio Interface 1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
40	SAI1	SAI1_MCLK	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE12
86	SAI1	SAI1_RX_BCLK	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH8
70	SAI1 and no WBRST	SAI1_RX_DATA0	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC10
117	SAI1 and no COEX	SAI1_RX_DATA1	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF10
72	SAI1	SAI1_RX_DATA2	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH9
75	SAI1	SAI1_RX_DATA3	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ8
122		SAI1_RX_DATA4	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD10
81		SAI1_RX_DATA5	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE10
71		SAI1_RX_DATA6	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH10
54		SAI1_RX_DATA7	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH12
81		SAI1_RX_SYNC	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE10
82	SAI1 and no WBRST	SAI1_RX_SYNC	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ9
40	SAI1	SAI1_TX_BCLK	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE12
57		SAI1_TX_BCLK	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ12
73		SAI1_TX_DATA0	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ11
70	SAI1	SAI1_TX_DATA1	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC10
177		SAI1_TX_DATA1	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ10
56		SAI1_TX_DATA2	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH11
55		SAI1_TX_DATA3	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD12
54		SAI1_TX_DATA4	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH12
113		SAI1_TX_DATA4	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH13
96		SAI1_TX_DATA5	0	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter	SOC.AH14
77	SAI and no COEX	SAI1_TX_DATA6	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC12
173	SAI1 and no WBRST	SAI1_TX_DATA7	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ13
54		SAI1_TX_SYNC	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH12

Pin#	Assy	Pin Function	Alt#	Notes	Ball
120		SAI1_TX_SYNC	0	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF12

8.9.2.2 SAI2 Signals

Table 29: Serial Audio Interface 2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
48		SAI2_MCLK	0	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	SAI2_MCLK	0	Dual pin, exported also on pin 48	SOC.AJ15
22		SAI2_RX_BCLK	0		SOC.AJ16
21		SAI2_RX_DATA0	0		SOC.AJ14
23		SAI2_RX_DATA1	3		SOC.AH17
196	no AC	SAI2_RX_DATA1	1	Available in SOM without "AC" configuration	SOC.AJ19
197	no AC	SAI2_RX_DATA2	1	Available in SOM without "AC" configuration	SOC.AJ18
198	no AC	SAI2_RX_DATA3	1	Available in SOM without "AC" configuration	SOC.AF18
23		SAI2_RX_SYNC	0		SOC.AH17
25		SAI2_TX_BCLK	0		SOC.AH15
26		SAI2_TX_DATA0	0		SOC.AH16
21		SAI2_TX_DATA1	3		SOC.AJ14
24		SAI2_TX_DATA1	3		SOC.AJ17
199	no AC	SAI2_TX_DATA1	1	Available in SOM without "AC" configuration	SOC.AC16
200	no AC	SAI2_TX_DATA2	1	Available in SOM without "AC" configuration	SOC.AH19
18	no AC	SAI2_TX_DATA3	1	Available in SOM without "AC" configuration	SOC.AH18
24		SAI2_TX_SYNC	0		SOC.AJ17

8.9.2.3 SAI3 Signals

Note: SAI3 interface is used by internal Audio Codec.
SAI3 interface can be used externally only in SOMs without “AC” assembly option.

Table 30: Serial Audio Interface 3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
20	no AC	SAI3_MCLK	0	Available in SOM without "AC” configuration	SOC.AJ20
48		SAI3_MCLK	6	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	SAI3_MCLK	6	Dual pin, exported also on pin 48	SOC.AJ15
79		SAI3_MCLK	2	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R26
197	no AC	SAI3_RX_BCLK	0	Available in SOM without "AC” configuration	SOC.AJ18
84	no SDEX	SAI3_RX_DATA0	2	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R25
198	no AC	SAI3_RX_DATA0	0	Available in SOM without "AC” configuration	SOC.AF18
196	no AC	SAI3_RX_DATA1	3	Available in SOM without "AC” configuration	SOC.AJ19
196	no AC	SAI3_RX_SYNC	0	Available in SOM without "AC” configuration	SOC.AJ19
145	QSPI	SAI3_TX_BCLK	2	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.N25
200	no AC	SAI3_TX_BCLK	0	Available in SOM without "AC” configuration	SOC.AH19
18	no AC	SAI3_TX_DATA0	0	Available in SOM without "AC” configuration	SOC.AH18
147	QSPI	SAI3_TX_DATA0	2	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.L26
199	no AC	SAI3_TX_DATA1	3	Available in SOM without "AC” configuration	SOC.AC16
31	QSPI	SAI3_TX_SYNC	2	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.L25
199	no AC	SAI3_TX_SYNC	0	Available in SOM without "AC” configuration	SOC.AC16

8.9.2.4 SAI5 Signals

Table 31: Serial Audio Interface 5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
Pin#	Assy	Pin Function	Alt#	Notes	Ball
20	no AC	SAI5_MCLK	2	Available in SOM without "AC" configuration	SOC.AJ20
48		SAI5_MCLK	1	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	SAI5_MCLK	1	Dual pin, exported also on pin 48	SOC.AJ15
197	no AC	SAI5_RX_BCLK	2	Available in SOM without "AC" configuration	SOC.AJ18
198	no AC	SAI5_RX_DATA0	2	Available in SOM without "AC" configuration	SOC.AF18
199	no AC	SAI5_RX_DATA1	2	Available in SOM without "AC" configuration	SOC.AC16
200	no AC	SAI5_RX_DATA2	2	Available in SOM without "AC" configuration	SOC.AH19
18	no AC	SAI5_RX_DATA3	2	Available in SOM without "AC" configuration	SOC.AH18
196	no AC	SAI5_RX_SYNC	2	Available in SOM without "AC" configuration	SOC.AJ19
22		SAI5_TX_BCLK	1		SOC.AJ16
21		SAI5_TX_DATA0	1		SOC.AJ14
23		SAI5_TX_DATA1	2		SOC.AH17
24		SAI5_TX_DATA1	1		SOC.AJ17
25		SAI5_TX_DATA2	1		SOC.AH15
26		SAI5_TX_DATA3	1		SOC.AH16
23		SAI5_TX_SYNC	1		SOC.AH17

8.9.2.5 SAI6 Signals

Table 32: Serial Audio Interface 6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
1	no EC	SAI6_MCLK	2	Referenced to pin 36 supply (1.8V/3.3V); On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
54		SAI6_MCLK	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH12
173	SAI1 and no WBRST	SAI6_MCLK	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ13
11	no EC	SAI6_RX_BCLK	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AC25
113		SAI6_RX_BCLK	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH13
122		SAI6_RX_BCLK	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD10
5	no EC	SAI6_RX_DATA0	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF26
81		SAI6_RX_DATA0	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE10
96		SAI6_RX_DATA0	1	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter	SOC.AH14
9	no EC	SAI6_RX_SYNC	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE26
71		SAI6_RX_SYNC	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH10
77	SAI1	SAI6_RX_SYNC	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC12
3	no EC	SAI6_TX_BCLK	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AD24
113		SAI6_TX_BCLK	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH13
122		SAI6_TX_BCLK	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD10
74		SAI6_TX_DATA0	2	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH28
81		SAI6_TX_DATA0	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE10
96		SAI6_TX_DATA0	2	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter	SOC.AH14
30		SAI6_TX_SYNC	2	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH29
71		SAI6_TX_SYNC	1	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH10
77	SAI and no COEX	SAI6_TX_SYNC	2	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC12

8.9.2.6 SAI7 Signals

Table 33: Serial Audio Interface 7 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
12	no EC	SAI7_MCLK	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF28
41		SAI7_MCLK	3		SOC.AH20
10	no EC	SAI7_RX_BCLK	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF29
52		SAI7_RX_BCLK	3	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AC20
4	no EC	SAI7_RX_DATA0	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG29
50		SAI7_RX_DATA0	3	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
6	no EC	SAI7_RX_SYNC	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG28
53		SAI7_RX_SYNC	3	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AF20
16	no EC	SAI7_TX_BCLK	2	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter	SOC.AE29
43		SAI7_TX_BCLK	3		SOC.AH21
45		SAI7_TX_DATA0	3		SOC.AJ21
58	no EC	SAI7_TX_DATA0	2	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AE24
15	no EC	SAI7_TX_SYNC	2	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE28
51		SAI7_TX_SYNC	3	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20

The following table details the SAI interface signals definition.

Table 34: SAI interface signals definition

Name	Function	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD	Receive Data. The receive data is sampled synchronously by the bit clock.	I

8.9.3 PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX 8M Plus SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

The PDM Microphone Interface module is composed of:

- An input interface for each pair of PDM microphones.
- A decimation filter by channel.
- A FIFO by channel.
- A time generation unit.
- Shared interfaces to DMA, interrupts and SoC.
- One or more Hardware Voice Activity Detectors (HWVAD).

PDM block main features are:

- Decimation filters:
    - Fixed filtering characteristics for audio application.
    - 24-bit signed filter output.
    - Maximum dynamic range: 120dB.
    - Internal clock divider for a programmable PDM clock generation.
    - Full or partial set of channels operation with individual enable control.
    - Programmable decimation rate.
    - Programmable DC remover.
    - Range adjustment capability.
    - FIFOs with interrupt and DMA capability.
        - Each FIFO with 32 entries length.
- Hardware Voice Activity Detector (HWVAD).
    - Interrupt capability.
    - Zero-Crossing Detection (ZCD) option.

Table 35: PDM Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
6	no EC	PDM_BIT_STREAM0	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG28
9	no EC	PDM_BIT_STREAM0	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE26
62		PDM_BIT_STREAM0	4	Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
70	SAI1 and no WBRST	PDM_BIT_STREAM0	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC10
196	no AC	PDM_BIT_STREAM0	6	Available in SOM without "AC" configuration	SOC.AJ19
4	no EC	PDM_BIT_STREAM1	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG29
5	no EC	PDM_BIT_STREAM1	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF26
22		PDM_BIT_STREAM1	6		SOC.AJ16
25		PDM_BIT_STREAM1	6		SOC.AH15
63		PDM_BIT_STREAM1	4	Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
117	SAI1 and no COEX	PDM_BIT_STREAM1	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF10
198	no AC	PDM_BIT_STREAM1	6	Available in SOM without "AC" configuration	SOC.AF18
3	no EC	PDM_BIT_STREAM2	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AD24
16	no EC	PDM_BIT_STREAM2	3	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter	SOC.AE29
23		PDM_BIT_STREAM2	6		SOC.AH17
24		PDM_BIT_STREAM2	6		SOC.AJ17
61		PDM_BIT_STREAM2	4	Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
72	SAI1 and no WBRST	PDM_BIT_STREAM2	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH9
200	no AC	PDM_BIT_STREAM2	6	Available in SOM without "AC" configuration	SOC.AH19
15	no EC	PDM_BIT_STREAM3	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE28
21		PDM_BIT_STREAM3	6		SOC.AJ14
30		PDM_BIT_STREAM3	3	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH29
65		PDM_BIT_STREAM3	4	Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
75	SAI and no COEX	PDM_BIT_STREAM3	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ8
199	no AC	PDM_BIT_STREAM3	6	Available in SOM without "AC" configuration	SOC.AC16
10	no EC	PDM_CLK	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF29
11	no EC	PDM_CLK	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AC25
64		PDM_CLK	4	Bank voltage set on SOM 1.8V/3.3V	SOC.AB28
86	SAI1 and no COEX	PDM_CLK	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH8

Pin#	Assy	Pin Function	Alt#	Notes	Ball
173	SAI1 and no WBRST	PDM_CLK	3	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ13
197	no AC	PDM_CLK	6	Available in SOM without "AC" configuration	SOC.AJ18

8.9.4 SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

Table 36: SPDIF Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		SPDIF1_EXT_CLK	0		SOC.AC18
18	no AC	SPDIF1_EXT_CLK	4	Available in SOM without "AC" configuration	SOC.AH18
12	no EC	SPDIF1_IN	3	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF28
20	no AC	SPDIF1_IN	6	Available in SOM without "AC" configuration	SOC.AJ20
65		SPDIF1_IN	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
196	no AC	SPDIF1_IN	4	Available in SOM without "AC" configuration	SOC.AJ19
1	no EC	SPDIF1_OUT	3	Referenced to pin 36 supply (1.8V/3.3V); On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
20	no AC	SPDIF1_OUT	4	Available in SOM without "AC" configuration	SOC.AJ20
61		SPDIF1_OUT	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
68		SPDIF1_OUT	0		SOC.AE18

8.10 Resistive Touch

The VAR-SOM-MX8M-PLUS features on board a 4-wire resistive touch panel interface controller (TI TSC2046) with the following features:

- Compatible with 4-wire resistive touch screens
- Pen-detection and nIRQ generation
- Supports several schemes of measurement, averaging to filter noise

The Resistive Touch is available only in SOMs with the “TP” assembly option
when not assembled, ECSPI1 SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

Note: *Resistive touch Controller cannot be assembled if WBE option is selected.*

8.10.1.1 Resistive Touch Signals

Table 37: Serial Resistive Touch Interface Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
187	TP	TS_X-		Signal source is Resistive Touch controller	TSC2046.8
189	TP	TS_X+		Signal source is Resistive Touch controller	TSC2046.6
191	TP	TS_Y+		Signal source is Resistive Touch controller	TSC2046.7
193	TP	TS_Y-		Signal source is Resistive Touch controller	TSC2046.9

8.11 UART

The VAR-SOM-MX8M-PLUS exposes up to four UART interfaces some of which are multiplexed with other peripherals. UART3 is used on SOM for Bluetooth interface and can be accessible only if the on SOM buffer is disabled or on SOM without ***"WBD" and "WB" Configuration***.

The UART includes the following features:

- High-speed TIA/EIA-232-F compatible, up to 5 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- DCE/DTE capability
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

Table 38: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

8.11.1 UART1 Signals

Table 39: UART1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
24		UART1_CTS_B	4		SOC.AJ17
44		UART1_CTS_B	1		SOC.AE6
31	SDEX	UART1_CTS_B	4	Pin referenced to 1.8V	SOC.Y28
21		UART1_RTS_B	4		SOC.AJ14
46		UART1_RTS_B	1		SOC.AJ4
84	SDEX	UART1_RTS_B	4	Pin referenced to 1.8V	SOC.Y29
22		UART1_RX	4		SOC.AJ16
175		UART1_RX	0		SOC.AD6
147	SDEX	UART1_RX	4	Pin referenced to 1.8V	SOC.W29
23		UART1_TX	4		SOC.AH17
124		UART1_TX	0		SOC.AJ3
145	SDEX	UART1_TX	4	Pin referenced to 1.8V	SOC.W28

8.11.2 UART2 Signals

Table 40: UART2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
115		UART2_CTS_B	1		SOC.AJ5
197	no AC	UART2_CTS_B	4	Available in SOM without "AC" configuration	SOC.AJ18
171		UART2_RTS_B	1		SOC.AH5
198	no AC	UART2_RTS_B	4	Available in SOM without "AC" configuration	SOC.AF18
62		UART2_RX	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
83		UART2_RX	0	Used as debug UART on Variscite base board	SOC.AF6
199	no AC	UART2_RX	4	Available in SOM without "AC" configuration	SOC.AC16
35	SDEX	UART2_RX	4	Pin referenced to 1.8V	SOC.V28
63		UART2_TX	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
85		UART2_TX	0	Used as debug UART on Variscite base board	SOC.AH4
200	no AC	UART2_TX	4	Available in SOM without "AC" configuration	SOC.AH19
33	SDEX	UART2_TX	4	Pin referenced to 1.8V	SOC.V29

8.11.3 UART3 Signals

Table 41: UART3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		UART3_CTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
51		UART3_RTS_B	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20
44		UART3_RX	0		SOC.AE6
53		UART3_RX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AF20
145	QSPI	UART3_RX	4	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N25
46		UART3_TX	0		SOC.AJ4
52		UART3_TX	1	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AC20

8.11.4 UART4 Signals

Table 42: UART4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
33	QSPI	UART4_CTS_B	3	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L24
41		UART4_CTS_B	1		SOC.AH20
35	QSPI	UART4_RTS_B	3	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N24
39		UART4_RTS_B	1		SOC.AJ22
43		UART4_RX	1		SOC.AH21
60		UART4_RX	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
84		UART4_RX	4	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R25
115		UART4_RX	0		SOC.AJ5
31	QSPI	UART4_TX	4	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L25
45		UART4_TX	1		SOC.AJ21
64		UART4_TX	3	Bank voltage set on SOM 1.8V/3.3V	SOC.AB28
171		UART4_TX	0		SOC.AH5

8.12 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.

Note: CAN-FD is supported only on Industrial variant of the SOM, Consumer variant of the SOM supports only CAN

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

8.12.1 FLEXCAN1 Signals

Table 43: FLEXCAN1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
25		FLEXCAN1_RX	3		SOC.AH15
176		FLEXCAN1_RX	4	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AF22
22		FLEXCAN1_TX	3		SOC.AJ16
68		FLEXCAN1_TX	4		SOC.AE18
174		FLEXCAN1_TX	4	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AC22

8.12.2 FLEXCAN2 Signals

Table 44: FLEXCAN2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
46		FLEXCAN2_RX	4		SOC.AJ4
48		FLEXCAN2_RX	3	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	FLEXCAN2_RX	3	Dual pin, exported also on pin 48	SOC.AJ15
154	no CSI2	FLEXCAN2_RX	4	Available in SOM without "CSI2" configuration	SOC.AE22
26		FLEXCAN2_TX	3		SOC.AH16
44		FLEXCAN2_TX	4		SOC.AE6
156	no CSI2	FLEXCAN2_TX	4	Available in SOM without "CSI2" configuration	SOC.AD22

8.13 ECSPI - Enhanced Configurable SPI

The VAR-SOM-MX8M-PLUS exposes all ECSPI interfaces.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:

- Full-duplex synchronous serial interface
- Master/Slave configurable
- One native Chip Select (SS) signal [see note below]
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Refer to the product data sheet for the maximum operating frequency

Note: Note: For interacting multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select. Examples can be found in our DTS files.

8.13.1 ESCPI1 Signals

Note: ECSPI1 interface is used by internal Resistive Touch Controller.
ECSPI1 interface can be used externally only in SOMs without “TP” assembly option.

Table 45: ECSPI1 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		ECSPI1_MISO	0	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
193	no TP	ECSPI1_MISO	3	Available in SOM without TP	SOC.AH6
52		ECSPI1_MOSI	0	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AC20
187	no TP	ECSPI1_MOSI	3	Available in SOM without TP	SOC.AH7
53		ECSPI1_SCLK	0	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AF20
189	no TP	ECSPI1_SCLK	3	Available in SOM without TP	SOC.AC8
51		ECSPI1_SS0	0	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20
191	no TP and no WBE	ECSPI1_SS0	3	Available in SOM without TP	SOC.AE8

8.13.2 ESCPI2 Signals

Table 46: ECSPI2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		ECSPI2_MISO	0		SOC.AH20
65		ECSPI2_MISO	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
92		ECSPI2_MISO	3		SOC.AF8
45		ECSPI2_MOSI	0		SOC.AJ21
64		ECSPI2_MOSI	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AB28
87		ECSPI2_MOSI	3		SOC.AJ6
43		ECSPI2_SCLK	0		SOC.AH21
60		ECSPI2_SCLK	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
88		ECSPI2_SCLK	3		SOC.AJ7
39		ECSPI2_SS0	0		SOC.AJ22
61		ECSPI2_SS0	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
90		ECSPI2_SS0	3		SOC.AD8

8.13.3 ESCPI3 Signals

Table 47: ECSPI3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
83		ECSPI3_MISO	1	Used as debug UART on Variscite base board	SOC.AF6
85		ECSPI3_SS0	1	Used as debug UART on Variscite base board	SOC.AH4
124		ECSPI3_MOSI	1		SOC.AJ3
175		ECSPI3_SCLK	1		SOC.AD6

8.14 QSPI/FlexSPI - Quad Serial Peripheral Interface

The VAR-SOM-MX8M-PLUS exposes one QSPI module which can be used to interface external serial flash devices.

The module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master

Note: QSPI signals are available on SOM with “QSPI” assembly option.
QSPI signals are referenced to 1.8v.

8.14.1 QSPIA Signals

Table 48: QSPIA Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
84	no SDEX	QSPI_A_DATA0	1	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R25
31	QSPI	QSPI_A_DATA1	1	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.L25
33	QSPI	QSPI_A_DATA2	1	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.L24
35	QSPI	QSPI_A_DATA3	1	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.N24
79		QSPI_A_DQS	1	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R26
145	QSPI	QSPI_A_SCLK	1	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.N25
147	QSPI	QSPI_A_SS0_B	1	Available in SOM with "QSPI” configuration; Pin referenced to 1.8V	SOC.L26

8.15 PWM

The VAR-SOM-MX8M-PLUS exports up to 4 General purpose Pulse Width Modulators (PWM) signals.

PWM Features:

- 16-bit up-counter with clock source selection (bus clock, baud clock, or 32K)
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

8.15.1 PWM Signals

Table 49: PWM Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
17		PWM1_OUT	1		SOC.AC18
75	no SAI1 and no COEX	PWM1_OUT	1		SOC.E8
77	no SAI1 and no COEX	PWM1_OUT	2		SOC.A8
90		PWM1_OUT	1		SOC.AD8
69		PWM2_OUT	2		SOC.D8
70	no SAI1	PWM2_OUT	5		SOC.A6
92		PWM2_OUT	1		SOC.AF8
173	no SAI1 and no WBRST	PWM2_OUT	2		SOC.B8
68		PWM3_OUT	1		SOC.AE18
80		PWM3_OUT	5		SOC.A4
87		PWM3_OUT	1		SOC.AJ6
20	no AC	PWM4_OUT	1	Available in SOM without "AC" configuration	SOC.AJ20
29		PWM4_OUT	5		SOC.B5
88		PWM4_OUT	1		SOC.AJ7

8.16 I2C

The VAR-SOM-MX8M-PLUS exposes up to 5x I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:

- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
    - Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
    - In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

8.16.1 I2C1 Signals

I2C1 is used internally by on-SOM EEPROM used for boot process and by Audio codec.
Using it externally from SOM pins with have the I2C1 alternate function in not allowed.

8.16.2 I2C2 Signals

Table 50: I2C2 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
50		I2C2_SCL	2	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
193	no TP	I2C2_SCL	0	Available in SOM without TP	SOC.AH6
51		I2C2_SDA	2	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20
191	no TP and	I2C2_SDA	0	Available in SOM without TP	SOC.AE8

Pin#	Assy	Pin Function	Alt#	Notes	Ball
	no WBE				

8.16.3 I2C3 Signals

Table 51: I2C3 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
43		I2C3_SCL	2		SOC.AH21
79		I2C3_SCL	4	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R26
88		I2C3_SCL	0		SOC.AJ7
45		I2C3_SDA	2		SOC.AJ21
87		I2C3_SDA	0		SOC.AJ6

8.16.4 I2C4 Signals

Table 52: I2C4 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		I2C4_SCL	2		SOC.AH20
63		I2C4_SCL	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
92		I2C4_SCL	0		SOC.AF8
33	SDEX	I2C4_SCL	3	Pin referenced to 1.8V	SOC.V29
33	QSPI	I2C4_SDA	4	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L24
39		I2C4_SDA	2		SOC.AJ22
62		I2C4_SDA	2	Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
90		I2C4_SDA	0		SOC.AD8
35	SDEX	I2C4_SDA	3	Pin referenced to 1.8V	SOC.V28

8.16.5 I2C5 Signals

Table 53: I2C5 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
68		I2C5_SCL	2		SOC.AE18
174		I2C5_SCL	3	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AC22
145	SDEX	I2C5_SCL	3	Pin referenced to 1.8V	SOC.W28
176		I2C5_SDA	3	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AF22
147	SDEX	I2C5_SDA	3	Pin referenced to 1.8V	SOC.W29

8.16.6 I2C6 Signals

Table 54: I2C6 Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
115		I2C6_SCL	4		SOC.AJ5
156	no CSI2	I2C6_SCL	3	Available in SOM without "CSI2" configuration	SOC.AD22
84	SDEX	I2C6_SCL	3	Pin referenced to 1.8V	SOC.Y29
154	no CSI2	I2C6_SDA	3	Available in SOM without "CSI2" configuration	SOC.AE22
171		I2C6_SDA	4		SOC.AH5
31	SDEX	I2C6_SDA	3	Pin referenced to 1.8V	SOC.Y28

8.17 General Purpose Timer

The VAR-SOM-MX8M-PLUS exposes the GPT interface to its connector.

GPT Features include:

- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

8.17.1.1 GPT Signals

Table 55: General Purpose Timer Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
171		GPT1_CAPTURE1	3		SOC.AH5
200	no AC	GPT1_CAPTURE1	3	Available in SOM without "AC" configuration	SOC.AH19
18	no AC	GPT1_CAPTURE2	3	Available in SOM without "AC" configuration	SOC.AH18
44		GPT1_CAPTURE2	3		SOC.AE6
46		GPT1_CLK	3		SOC.AJ4
197	no AC	GPT1_CLK	3	Available in SOM without "AC" configuration	SOC.AJ18
68		GPT1_COMPARE1	3		SOC.AE18
115		GPT1_COMPARE1	3		SOC.AJ5
85		GPT1_COMPARE2	3	Used as debug UART on Variscite base board	SOC.AH4
17		GPT1_COMPARE3	3		SOC.AC18
83		GPT1_COMPARE3	3	Used as debug UART on Variscite base board	SOC.AF6
88		GPT2_CLK	2		SOC.AJ7
87		GPT3_CLK	2		SOC.AJ6

8.18 Reference Clocks

The VAR-SOM-MX8 exposes the clock outputs from the internal CCM module which can be used to clock external devices.

8.18.1 Clock Signals

Table 56: Clock Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
41		CCM_CLKO1	4		SOC.AH20
80		CCM_CLKO1	6		SOC.A4
29		CCM_CLKO2	6		SOC.B5
39		CCM_CLKO2	4		SOC.AJ22
40	no SAI1	CCM_ENET_PHY_REF_CLK_ROOT	1	Differential Pair Positive side	SOC.A7
40	no SAI1	CCM_EXT_CLK1	6		SOC.A7
75	no SAI1 and no COEX	CCM_EXT_CLK2	6		SOC.E8
86	no SAI1 and no COEX	CCM_EXT_CLK3	6		SOC.A3
82	no SAI1 and no WBRST	CCM_EXT_CLK4	6		SOC.F6
69		CCM_PMIC_READY	5	Differential Pair Positive side	SOC.D8
72	no SAI1	CCM_PMIC_READY	5	Differential Pair Positive side	SOC.B4
75	no SAI1 and no COEX	CCM_REF_CLK_24M	5		SOC.E8
40	no SAI1	CCM_REF_CLK_32K	5		SOC.A7
5	no EC	ENET_QOS_INPUT=ENET_ QOS_TX_CLK OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT	1	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF26
40	SAI1	ENET1_INPUT=ENET1_TX_ CLK OUTPUT=CCM_ENET_REF_ CLK_ROOT	4	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE12

8.19 JTAG

The VAR-SOM-MX8M-PLUS consists of the the System JTAG Controller (SJC) provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG) and IEEE 1149.6 standards.

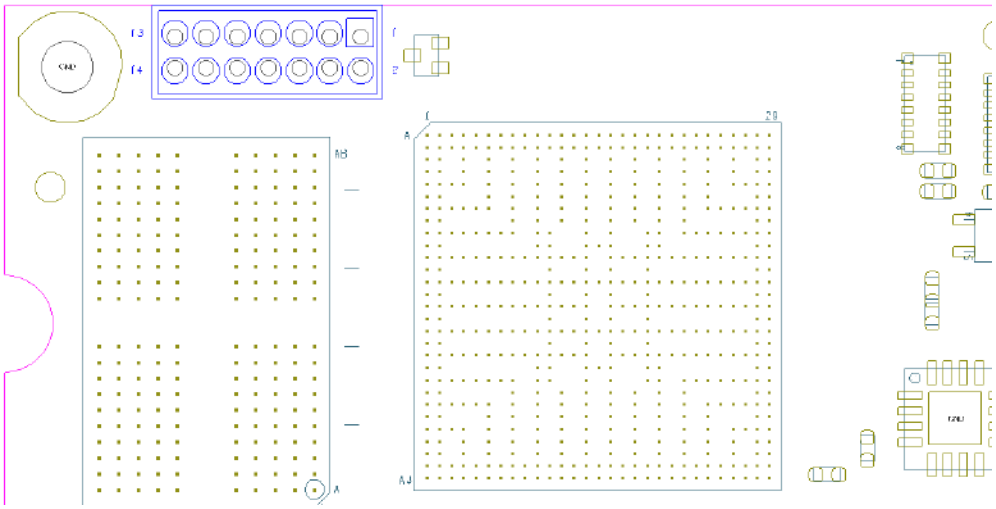
The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG.
JTAG port interfaces the M7 and Cortex A53 Cores DAP - debug access port.
The VAR-SOM-MX8M-PLUS JTAG MOD pin is hardware tied low and enables the Daisy chain ALL mode only, used for common SW debug (High speed and production).

VAR-SOM-MX8M-PLUS exposes JTAG signals on a 14-pin header (not assembled by default) on the SOM top left side. Pins 1-10 are dedicated for JTAG pins, pins 11-14 are dedicated for BOOT_MODE pins (see “boot configuration” section).

8.19.1 JTAG Signals

Table 57: JTAG signals on 14-pin Header Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
1		JTAG_VTREF		JTAG reference voltage (3.3v)	
2		JTAG_TMS		JTAG Test Mode select	SOC.G14
3		GND		Digital Ground	
4		JTAG_TCK		JTAG Test Clock	SOC.G18
5		GND		Digital Ground	
6		JTAG_TDO		JTAG Test Data Out	SOC.F14
7		RTCK		JTAG Return clock	
8		JTAG_TDI		JTAG Test Data In	SOC.G16
9		GND		Digital Ground	
10		JTAG_SRST_B		JTAG System reset	



8.20 General Purpose IO

The VAR-SOM-MX8M-PLUS provides IO pins which can be used as GPIOs.

8.20.1 GPIO Signals

Table 58: GPIO Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
40	no SAI1	GPIO1_IO00	0		SOC.A7
75	no SAI1 and no COEX	GPIO1_IO01	0		SOC.E8
117	no SAI1 and no COEX	GPIO1_IO03	0		SOC.D6
72	no SAI1 and no WBRST	GPIO1_IO05	0		SOC.B4
86	no SAI1 and no COEX	GPIO1_IO06	0		SOC.A3
82	no SAI1 and no WBRST	GPIO1_IO07	0		SOC.F6
77	no SAI1 and no COEX	GPIO1_IO08	0		SOC.A8
173	no SAI1 and no WBRST	GPIO1_IO09	0		SOC.B8
69		GPIO1_IO11	0		SOC.D8
70	no SAI1 and no WBRST	GPIO1_IO13	0		SOC.A6
80		GPIO1_IO14	0		SOC.A4
29		GPIO1_IO15	0		SOC.B5
74		GPIO1_IO16	5	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH28
30		GPIO1_IO17	5	Shared by SOM with "EC"; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC" configuration	SOC.AH29
3	no EC	GPIO1_IO18	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AD24
5	no EC	GPIO1_IO19	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF26
9	no EC	GPIO1_IO20	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE26

Pin#	Assy	Pin Function	Alt#	Notes	Ball
11	no EC	GPIO1_IO21	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AC25
1	no EC	GPIO1_IO22	5	Referenced to pin 36 supply (1.8V/3.3V); On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AF24
58	no EC	GPIO1_IO23	5	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter; On some SOM modules this pin is GND; If placed in such carrier with no "EC" configuration define PAD as input!	SOC.AE24
15	no EC	GPIO1_IO24	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AE28
16	no EC	GPIO1_IO25	5	Referenced to pin 36 supply (1.8V/3.3V); Includes series EMI filter	SOC.AE29
4	no EC	GPIO1_IO26	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG29
6	no EC	GPIO1_IO27	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AG28
10	no EC	GPIO1_IO28	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF29
12	no EC	GPIO1_IO29	5	Referenced to pin 36 supply (1.8V/3.3V)	SOC.AF28
145	SDEX	GPIO2_IO00	5	Pin referenced to 1.8V	SOC.W28
147	SDEX	GPIO2_IO01	5	Pin referenced to 1.8V	SOC.W29
84	SDEX	GPIO2_IO02	5	Pin referenced to 1.8V	SOC.Y29
31	SDEX	GPIO2_IO03	5	Pin referenced to 1.8V	SOC.Y28
33	SDEX	GPIO2_IO04	5	Pin referenced to 1.8V	SOC.V29
35	SDEX	GPIO2_IO05	5	Pin referenced to 1.8V	SOC.V28
60		GPIO2_IO13	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
64		GPIO2_IO14	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AB28
62		GPIO2_IO15	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
63		GPIO2_IO16	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
61		GPIO2_IO17	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
65		GPIO2_IO18	5	Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
145	QSPI	GPIO3_IO00	5	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N25
147	QSPI	GPIO3_IO01	5	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L26
84	no SDEX	GPIO3_IO06	5	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R25
31	QSPI	GPIO3_IO07	5	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L25
33	QSPI	GPIO3_IO08	5	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.L24
35	QSPI	GPIO3_IO09	5	Available in SOM with "QSPI" configuration; Pin referenced to 1.8V	SOC.N24
79		GPIO3_IO14	5	Pin is routed by default via on SOM 1.8<->3.3V open drain voltage translator with 10K Pull up. In "QSPI" configuration Pin is routed directly from CPU @1.8v	SOC.R26
174		GPIO3_IO26	5	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AC22

Pin#	Assy	Pin Function	Alt#	Notes	Ball
176		GPIO3_IO27	5	Internal signal pulled up to SOM_PER_3V3 using 10K resistor;	SOC.AF22
156	no CSI2	GPIO3_IO28	5	Available in SOM without "CSI2" configuration	SOC.AD22
154	no CSI2	GPIO3_IO29	5	Available in SOM without "CSI2" configuration	SOC.AE22
82	SAI1 and no WBRST	GPIO4_IO00	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ9
86	SAI1 and no COEX	GPIO4_IO01	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH8
70	SAI1	GPIO4_IO02	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC10
117	SAI1 and no COEX	GPIO4_IO03	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF10
72	SAI1	GPIO4_IO04	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH9
75	SAI and no COEX	GPIO4_IO05	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ8
122		GPIO4_IO06	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD10
81		GPIO4_IO07	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE10
71		GPIO4_IO08	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH10
54		GPIO4_IO09	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH12
120		GPIO4_IO10	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AF12
57		GPIO4_IO11	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ12
73		GPIO4_IO12	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ11
177		GPIO4_IO13	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ10
56		GPIO4_IO14	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH11
55		GPIO4_IO15	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AD12
113		GPIO4_IO16	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AH13
96		GPIO4_IO17	5	Referenced to pin 38 supply (1.8V/3.3V) Includes series EMI filter	SOC.AH14
77	SAI and no COEX	GPIO4_IO18	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AC12
173	SAI1 and no WBRST	GPIO4_IO19	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AJ13
40	SAI1	GPIO4_IO20	5	Referenced to pin 38 supply (1.8V/3.3V)	SOC.AE12
23		GPIO4_IO21	5		SOC.AH17
22		GPIO4_IO22	5		SOC.AJ16
21		GPIO4_IO23	5		SOC.AJ14
24		GPIO4_IO24	5		SOC.AJ17
25		GPIO4_IO25	5		SOC.AH15
26		GPIO4_IO26	5		SOC.AH16

Pin#	Assy	Pin Function	Alt#	Notes	Ball
48		GPIO4_IO27	5	Dual pin, exported also on pin 191 in no TP and WBE	SOC.AJ15
191	no TP and WBE	GPIO4_IO27	5	Dual pin, exported also on pin 48	SOC.AJ15
196	no AC	GPIO4_IO28	5	Available in SOM without "AC" configuration	SOC.AJ19
197	no AC	GPIO4_IO29	5	Available in SOM without "AC" configuration	SOC.AJ18
198	no AC	GPIO4_IO30	5	Available in SOM without "AC" configuration	SOC.AF18
199	no AC	GPIO4_IO31	5	Available in SOM without "AC" configuration	SOC.AC16
200	no AC	GPIO5_IO00	5	Available in SOM without "AC" configuration	SOC.AH19
18	no AC	GPIO5_IO01	5	Available in SOM without "AC" configuration	SOC.AH18
20	no AC	GPIO5_IO02	5	Available in SOM without "AC" configuration	SOC.AJ20
68		GPIO5_IO03	5		SOC.AE18
17		GPIO5_IO05	5		SOC.AC18
53		GPIO5_IO06	5	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AF20
52		GPIO5_IO07	5	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AC20
50		GPIO5_IO08	5	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AD20
51		GPIO5_IO09	5	Used internally with "WBD", Function can be released if BT Function disabled Always exposed;	SOC.AE20
43		GPIO5_IO10	5		SOC.AH21
45		GPIO5_IO11	5		SOC.AJ21
41		GPIO5_IO12	5		SOC.AH20
39		GPIO5_IO13	5		SOC.AJ22
189	no TP	GPIO5_IO14	5	Available in SOM without TP	SOC.AC8
187	no TP	GPIO5_IO15	5	Available in SOM without TP	SOC.AH7
193	no TP	GPIO5_IO16	5	Available in SOM without TP	SOC.AH6
191	no TP and no WBE	GPIO5_IO17	5	Available in SOM without TP	SOC.AE8
88		GPIO5_IO18	5		SOC.AJ7
87		GPIO5_IO19	5		SOC.AJ6
92		GPIO5_IO20	5		SOC.AF8
90		GPIO5_IO21	5		SOC.AD8
175		GPIO5_IO22	5		SOC.AD6
124		GPIO5_IO23	5		SOC.AJ3
83		GPIO5_IO24	5	Used as debug UART on Variscite base board	SOC.AF6
85		GPIO5_IO25	5	Used as debug UART on Variscite base board	SOC.AH4

Pin#	Assy	Pin Function	Alt#	Notes	Ball
44		GPIO5_IO26	5		SOC.AE6
46		GPIO5_IO27	5		SOC.AJ4
115		GPIO5_IO28	5		SOC.AJ5
171		GPIO5_IO29	5		SOC.AH5

8.21 Power

8.21.1 Power

Table 59: Power

Pin#	Assy	Pin Function	Alt#	Notes	Ball
32, 34, 103, 105, 107, 109, 111		VCC_SOM		SOM Power	VCC_SOM
36	no EC	VDD_ENET0_1P8_3P3_IN		ENET_QOS pins group power IN "EC" configuration: * Not Connected No "EC" configuration: NVCC_ENET 1.8V/3.3V supply voltage input. The following SOM pins are referenced to this voltage: 1,3,4,5,6,9,10,11,12,15,16,30,58,74. Must supply one option: * For RMII - connect to 1.8 or 3.3V. * For RGMII - connect to 1.8V * For other alternates - connect to 1.8V/3.3V	VDD_ENET0_1P8_3P3_IN
38		VDD_ENET1_1P8_3P3_IN		ENET1 pins group power IN NVCC_SAI1_SAI5 supply voltage input. The following SOM pins are referenced to this voltage: 54,55,56,57,71,73,81,96,113,120,122,177 In "SAI1" configuration, also these pins are referenced to this voltage: 40,70,72,75,77,82,86,117,173 Must supply one option: * For RMII - connect to 1.8 or 3.3V. * For RGMII - connect to 1.8V * For other alternates - connect to 1.8V/3.3V	VDD_ENET1_1P8_3P3_IN
104		USB2_VBUS	0	USB Host VBUS (5V) input	SOC.D12
106		USB1_VBUS	0	USB Host VBUS (5V) input	SOC.A11
49		SOM_3V3_PER		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_3V3_PER

8.21.2 Ground

Table 60: Digital Ground Pins

Pin#	Assy	Pin Function	Alt#	Notes	Ball
2, 7, 8, 13, 14, 19, 27, 28, 37, 47, 59, 66, 67, 76, 78, 89, 95, 101, 112, 118, 126, 132, 138, 139, 144, 149, 158, 159, 169, 172, 178, 179, 185		GND		Digital ground	GND
195	AGND			Audio ground	AGND

8.22 General System Control

8.22.1 General System Control Signals

Table 61: General System Control Signals

Pin#	Assy	Pin Function	Alt#	Notes	Ball
49		SOM_3V3_PER		SOM Peripherals' 3.3v rail Output. Should be used to sequence carrier board peripherals' 3.3v supply. Refer to Symphony-Board schematics for implementation. Max. 200mA current draw is allowed.	SOM_3V3_PER
98		SYS_nRST_3V3		SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset. By default cold reset is performed power cycling the PMIC rails. Can be programmed to perform warm reset instead.	PMIC.8

NOTE

Users using SOM_3V3_PER as a supply power source, required to add 10uF to 20uF ceramic capacitor rated to > 6.3V.

8.22.2 Boot configuration

The VAR-SOM-MX8M-PLUS can be boot from the following sources:

- Internal source - eMMC Flash memory
- External source - SD Card

The BOOT_MODE pins determine the boot source. On the SOM, BOOT_MODE [3:0] pins are strapped internally by 10K PU/PD resistors.
Boot source selection is done via **pin 42** of the SOM-DIMM 200 pin connector.

Table 62: BOOT_SEL signal SOM-DIMM 200 pin connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
42		BOOT_SEL		Controls internal OR external boot source; Internal signal pulled up to SOM_PER_3V3 using 10K resistor; 0=EXT. BOOT 1/Float=INT. BOOT	INT. LOGIC

(Note: On SOM, pin 42 signal is pulled up to SOM_PER_3V3 using 10K resistor and is connected to the Gate of an inverting FET which drives BOOT_MODE0 signal. This inversion is required in order to maintain "VAR-SOM" pin2pin family boot logic.)

BOOT_MODE[3:0] are also exposed on JTAG Header (not assembled by default) in order to allow support of other boot source.

Table 63: BOOT_MODE signals on 14-pin Header Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
11		BOOT_MODE0		Includes 10K PD resistor on SOM	SOC.G10
12		BOOT_MODE1		Includes 10K PU resistor on SOM	SOC.F8
13		BOOT_MODE2		Includes 10K PD resistor on SOM	SOC.G8
14		BOOT_MODE3		Includes 10K PD resistor on SOM	SOC.G12

Table 64: BOOT_MODE signals on SO-DIMM 200 pin Connector

Pin#	Assy	Pin Function	Alt#	Notes	Ball
26		SRC_BOOT_MODE4	6		SOC.AH16
18	no AC	SRC_BOOT_MODE5	6	Available in SOM without "AC" configuration	SOC.AH18

ATTENTION

External drivers connected to BOOT_MODE pins should be disabled on during reset (SYS_nRST_3V3), otherwise they may change the boot option and the SOM will not boot.

9. Assembly Options

To make the solution as Flexible as possible the following assembly options were added. The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1 DSI

The SOM can be ordered with the DSI related pins exposed.

Table 65: DSI assembly option

	Default SOM option (no DSI)		Special SOM option (DSI)	
Pin #	Pin Function	Ball	Pin Function	Ball
168	LVDS0_CLK_N	SOC.G28	MIPI_DSI1_CLK_N	SOC.B18
170	LVDS0_CLK_P	SOC.F29	MIPI_DSI1_CLK_P	SOC.A18
161	LVDS0_D0_N	SOC.E28	MIPI_DSI1_D0_N	SOC.B16
163	LVDS0_D0_P	SOC.D29	MIPI_DSI1_D0_P	SOC.A16
160	LVDS0_D1_N	SOC.F28	MIPI_DSI1_D1_N	SOC.B17
162	LVDS0_D1_P	SOC.E29	MIPI_DSI1_D1_P	SOC.A17
164	LVDS0_D2_N	SOC.H28	MIPI_DSI1_D2_N	SOC.B19
166	LVDS0_D2_P	SOC.G29	MIPI_DSI1_D2_P	SOC.A19
165	LVDS0_D3_N	SOC.J28	MIPI_DSI1_D3_N	SOC.B20
167	LVDS0_D3_P	SOC.H29	MIPI_DSI1_D3_P	SOC.A20

9.2 CSI2

The SOM can be ordered with the CSI2 related pins exposed.

Table 66: CSI2 assembly option

	Default SOM option (no CSI2)		Special SOM option (CSI2)	
Pin #	Pin Function	Ball	Pin Function	Ball
150	HDMI_TXC_N	SOC.AJ24	MIPI_CSI2_CLK_N	SOC.B23
152	HDMI_TXC_P	SOC.AH24	MIPI_CSI2_CLK_P	SOC.A23
157	HDMI_TX0_N	SOC.AJ25	MIPI_CSI2_D0_N	SOC.B25
155	HDMI_TX0_P	SOC.AH25	MIPI_CSI2_D0_P	SOC.A25
148	HDMI_TX1_N	SOC.AJ26	MIPI_CSI2_D1_N	SOC.B24
146	HDMI_TX1_P	SOC.AH26	MIPI_CSI2_D1_P	SOC.A24
153	HDMI_TX2_N	SOC.AJ27	MIPI_CSI2_D2_N	SOC.B22
151	HDMI_TX2_P	SOC.AH27	MIPI_CSI2_D2_P	SOC.A22
156	HDMI_CEC	SOC.AD22	MIPI_CSI2_D3_N	SOC.B21
154	HDMI_HPD	SOC.AE22	MIPI_CSI2_D3_P	SOC.A21

9.3 SAI1

The SOM can be ordered with related SAI1 pins exposed.
Alternatively, special assembly options COEX, WBRST can be exported on these pins.

Table 67: SAI1 assembly option

	Default SOM option (no SAI1, no COEX, no WBRST)		Special SOM option (SAI1, no COEX, no WBRST)	
Pin #	**Pin Function**	**Ball**	**Pin Function**	**Ball**
40	GPIO1_IO00	SOC.A7	SAI1_MCLK	SOC.AE12
70	GPIO1_IO13	SOC.A6	SAI1_RX_DATA0	SOC.AC10
72	GPIO1_IO05	SOC.B4	SAI1_RX_DATA2	SOC.AH9
75	GPIO1_IO01	SOC.E8	SAI1_RX_DATA3	SOC.AJ8
77	GPIO1_IO08	SOC.A8	SAI1_TX_DATA6	SOC.AC12
82	GPIO1_IO07	SOC.F6	SAI1_RX_SYNC	SOC.AJ9
86	GPIO1_IO06	SOC.A3	SAI1_RX_BCLK	SOC.AH8
117	GPIO1_IO03	SOC.D6	SAI1_RX_DATA1	SOC.AF10
173	GPIO1_IO09	SOC.B8	SAI1_TX_DATA7	SOC.AJ13

9.4 COEX

In case of WBD/WBE assembly, Wi-Fi COEX pins can be exported instead of pins used by “no SAI1”/” SAI1” assembly options.

	Special SOM option (COEX)	
Pin #	**Pin Function**	**Ball**
75	WCI-2_OUT (@1.8V)	LBES5PL2xL.70
77	NC	NC_COEX
86	NC	NC_COEX
117	WCI-2_SIN (@1.8V)	LBES5PL2xL.69

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.5 WBRST

In case of WBD/WBE assembly, Wi-Fi WBRST pins can be exported instead of pins used by “no SAI1”/” SAI1 assembly options.

	Special SOM option (WBRST)	
Pin #	**Pin Function**	**Ball**
70	IND_RST_BT (@1.8V)	LBES5PL2xL.64
72	NC	NC_WBRST
82	IND_RST_WL (@1.8V)	LBES5PL2xL.63
173	IND_RST_15.4 (@1.8V)	LBES5PL2xL.38

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.6 ANT2

In case of WBD/WBE assembly, The SOM can be ordered with Dual antennas. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.7 BTPCM

In case of WBD/WBE assembly, the SOM can be ordered with SAI5 balls internally connected to Bluetooth PCM lines.

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.8 QSPI/SDEX

The SOM can be ordered with related QSPIA pins exposed.
If a WIFI module is not assembled on the SOM, the SOM, alternately, can be ordered with SD1 pins exported.

Table 68: QSPI assembly option

	Default SOM option (no QSPI)		Special SOM option (QSPI)		Special SOM option (SDEX)	
Pin #	Pin Function	Ball	Pin Function	Ball	Pin Function	Ball
84	QSPI_A_DATA0 (via on SOM 1.8<->3.3V voltage translator)	SOC.R25	QSPI_A_DATA0 (@1.8V)	SOC.R25	CONN_SD1_DATA0 (@1.8V)	SOC.Y29
31	NC	NC_QSPI	QSPI_A_DATA1 (@1.8V)	SOC.L25	CONN_SD1_DATA1 (@1.8V)	SOC.Y28
33	NC	NC_QSPI	QSPI_A_DATA2 (@1.8V)	SOC.L24	CONN_SD1_DATA2 (@1.8V)	SOC.V29
35	NC	NC_QSPI	QSPI_A_DATA3 (@1.8V)	SOC.N24	CONN_SD1_DATA3 (@1.8V)	SOC.V28
79	QSPI_A_DQS (via on SOM 1.8<->3.3V voltage translator)	SOC.R26	QSPI_A_DQS (@1.8V)	SOC.R26	QSPI_A_DQS (via on SOM 1.8<->3.3V voltage translator)	SOC.R26
145	EARC_N_HPD (@1.8V)	SOC.AH22	QSPI_A_SCLK (@1.8V)	SOC.N25	CONN_SD1_CLK (@1.8V)	SOC.W28
147	EARC_P_UTIL (@1.8V)	SOC.AJ23	QSPI_A_SS0_B (@1.8V)	SOC.L26	CONN_SD1_CMD (@1.8V)	SOC.W29

9.9 Ethernet PHY

The SOM can be ordered without Ethernet PHY chip assembled; it allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
when not assembled, SoC balls are exported to SOM connector instead of Ethernet interface pins.

9.10 Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
when not assembled, SoC balls are exported to SOM connector instead of Analog codec interface pins.

9.11 WBD/WBE - Dual band Wi-Fi and BT/BLE, 802.15.4 combo

The SOM can be ordered without the Dual band Wi-Fi and BT/BLE, 802.15.4 combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

9.12 Resistive Touch

The SOM can be ordered without Resistive Touch controller assembled. This allows reducing the overall cost of the product in case the Resistive Touch is not used.
when not assembled, SoC balls are exported to SOM connector instead of Resistive Touch interface pins.

Resistive touch Controller cannot be ordered with "WBE" option.

9.13 LPDDR4

The SOM can be ordered with different RAM size capacities, it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.14 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 69: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VCC_SOM	-0.3	3.6	V	
USB_OTG1_VBUS, USB_OTG2_VBUS	-0.3	5.25	V	
VDD_ENET0_1P8_3P3_IN, VDD_ENET1_1P8_3P3_IN	-0.3	3.8	V	
Vin/Vout input/output voltage range (GPIO Type Pins)	-0.3	OVDD+0.3		OVDD is the I/O supply voltage
ESD damage immunity Human Body Model (HBM)	--	+/-1000	V	JS-001-2017 Reference
ESD damage immunity Charge Device Model (CDM)	--	+/-250	V	JS-002-2018 Reference

10.2 Operating Conditions

Table 70: Operating Ranges

Parameter		Min.	Typ.	Max.	Unit
VCC_SOM		3.25	3.3	3.45	V
USB_OTG1_VBUS/ USB_OTG2_VBUS		4.75	5	5.25	V
VDD_ENET0_1P8_3P3_IN/ VDD_ENET1_1P8_3P3_IN	1.8	1.65	1.8	1.95	V
	3.3	3	3.3	3.6	

10.3 Peripheral Voltage Levels

Most of the peripheral interface lines used as inputs or output to the VAR-SOM-MX8M-PLUS uses 3.3V LVCMOS levels, except the following interfaces: SD2, ENET_QOS, ENET1, HDMI, PCIe, USB, MIPI-DSI, MIPI-CSI, LVDS.

***PCIe/HDMI/USB/MIPI-DSI/MIPI-CSI/LVDS*:** Interfaces follow a different standard since they are high-speed signals.

uSDHC2: (SDIO lines) interface IOs will change voltage between 3.3V and 1.8V depending on the SD card capabilities.
With other alternative function user can determine the voltage uSDHC2 IOs bank will be 1.8V or 3.3V;

ENET_QOS: interface available in case SOM is ordered **without "EC"** configuration. IOs will run according to the power fed to VDD_ENET0_1P8_3P3_IN (pin 36) (1.8V/3.3V).

ENET1: IOs will run according to the power fed to VDD_ENET1_1P8_3P3_IN (pin 38) (1.8V/3.3V)

10.4 Power Consumption

Table 71: VAR-SOM-MX8M-PLUS Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	3.334V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 ax 5GHz
Run	3.340V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	3.343V	TBD	TBD	Linux up
FHD video playback	3.339V	TBD	TBD	On 800x400 LCD
Standby	3.357V	TBD	TBD	Memory retention mode (Measured after 3 min, R54 on Symphony-Board removed)
Off (RTC)	3.447V	TBD	TBD	All power rails are Off, only Internal SoC RTC is powered

NOTE

Setup:
HW:
VAR-SOM-MX8MPQ_V2_1800C_4096R_16G_AC_EC_WBD_BTPCM_CT_REV2.0
SW: mx8mp-yocto-mickledore-6.1.36_2.1.0-v1.1

DISCLAIMER:

The power consumption measurements apply only to limited operation scenarios. Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

11. Environmental Specifications

Table 72: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 6183 Khrs	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes for mounting it to the carrier board which are plated holes and connected to GND.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use the following standoff:

Manufacturer: **MAC8**

PN: **TH-1.6-3.0-M2-B**

12.2 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SOM-MX8M family:

Variscite PN: VHP-VS8M

DISCLAIMER:
Implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

12.3 SOM Dimensions

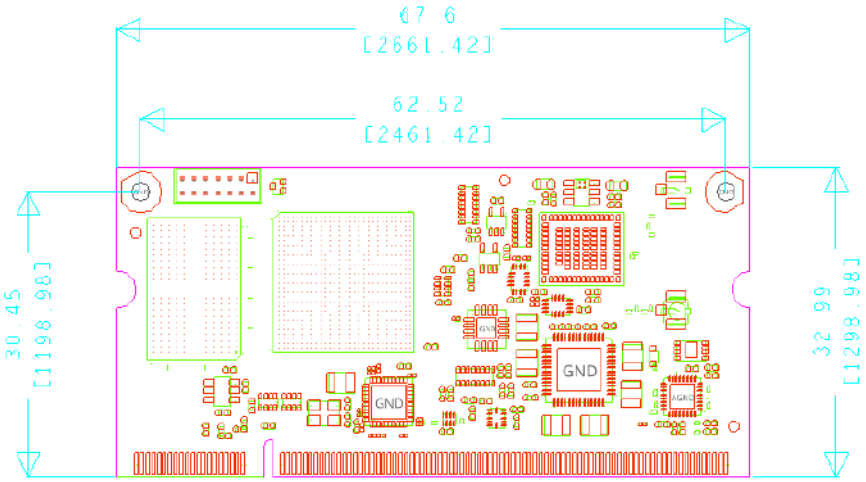


Figure 5: VAR-SOM-MX8M-PLUS Mechanics in millimeters [mils]

12.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

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