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VARISCITE LTD.

VAR-SMARC-MX8M-PLUS V1.x Datasheet
NXP i.MX 8M PLUS™ - based System-on-Module

VARISCITE LTD.

VAR-SMARC-MX8M-PLUS Datasheet

1. Document Revision History

Revision	Date	Notes
1.0	19/03/2026	Initial - preliminary

2.   Table of Contents

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4.   Overview

4.1   General Information

The VAR-SMARC-MX8M-PLUS offers a high-performance processing for a low-power System-on-Module.

The product is based on the i.MX 8M Plus family which is a set of NXP products focused on machine learning applications, combining state-of-art multimedia features with high-performance processing optimized for low-power consumption.

The Module is designed according to the SMARC ("Smart Mobility ARchitecture") 2.2 Specification.

The i.MX 8M Plus Media Applications Processor is built to achieve both high performance and low power consumption and relies on a powerful, fully coherent core complex based on a quad Cortex-A53 cluster and Cortex-M7 low-power coprocessor, audio digital signal processor, machine learning and graphics accelerators.

This heterogeneous multicore processing architecture enables the device to run an open operating system like Linux and an RTOS like FreeRTOS™ on the Cortex-M7 core for time and security critical tasks.

The VAR-SMARC-MX8M-PLUS provides an ideal building block for simple integration with a wide range of products in target markets requiring high-performance processing with low power consumption, compact size and a very cost-effective solution.

Supporting products:

- Echo-board – evaluation board

  - ✓ Carrier Board, compatible with VAR-SMARC-MX8M-PLUS
  - ✓ Schematics

- VAR-DVK-MX8MP SMARC full development kit, including:

  - ✓ Echo-board
  - ✓ VAR-SMARC-MX8M-PLUS
  - ✓ Display and touch
  - ✓ Accessories and cables

- O.S support
  - ✓ Linux BSP
  - ✓ Android

Contact Variscite support services for further information: support@variscite.com.

4.2 Feature Summary

- NXP i.MX8M-PLUS series SOC
    - o 4x Cortex A53 up to @ 1.8 GHz
    - o 1x Cortex M7 @ 800 MHz
    - o 1x Hi-Fi DSP @ 800 MHz
- Hardware 2D/3D Graphics Acceleration
    - o GC7000UltraLite 3D GPU (2 shaders) OpenGL ES 3.0, OpenCL1.2, Vulkan
    - o GC520L 2D GPU
- Machine Learning: NPU (Neural Processing Unit) 2.3 TOPS Neural Network performance
    - o Keyword detect, noise reduction, beamforming
    - o Speech recognition (i.e. Deep Speech 2)
    - o Image recognition (i.e. ResNet-50)
- Memory
    - o Up to 8GB LPDDR4 RAM @ 2000Mhz
    - o 8-bit up to 128GB eMMC boot and storage
- Display Support
    - o 2x LVDS interface 4-lane each
    - o HDMI 2.0a
    - o 1x MIPI DSI with up to 4 data lanes
- Networking
    - o 2x 10/100/1000 Mbit/s Ethernet Interface
    - o Certified Wi-Fi 802.11a/b/g/n/ac/ax
    - o Bluetooth: 5.4/BLE
- Camera
    - o Up to 2x MIPI CSI – CMOS Serial camera Interface 4 lanes
    - o 375 Mpixel/s HDR ISP (Image Sensor Processor)
- Audio
    - o Analog Stereo line in
    - o Analog headphones out
    - o Digital microphone
    - o Up to 6x Digital audio (SAI)
    - o 8-channel PDM microphone input
    - o SPDIF
- USB
    - o With HUB: 1x USB 2.0 OTG + 2x USB 2.0 HOST + 2x USB 3.0/2.0 HOST
    - o Without HUB: 1x USB 2.0 OTG + 1x USB 3.0/2.0 HOST
- Security
    - o TPM 2.0 device for Industrial devices
- RTC
    - o Real-Time Clock (RTC) and calendar
- Other Interfaces
    - o SDIO/MMC
    - o 1x PCIe v3.0
    - o Serial interfaces (ECSPI, FlexSPI, I2C, UART, CAN, JTAG)
    - o GPIOs
- Single power supply: 5V
- Dimensions (W x L x H):   82 mm x 50 mm x 3.5 mm
- Industrial temperature range: -40°C to 85°C

4.3   Block Diagram

Figure 1 : VAR-SMARC-MX8M-PLUS Block Diagram
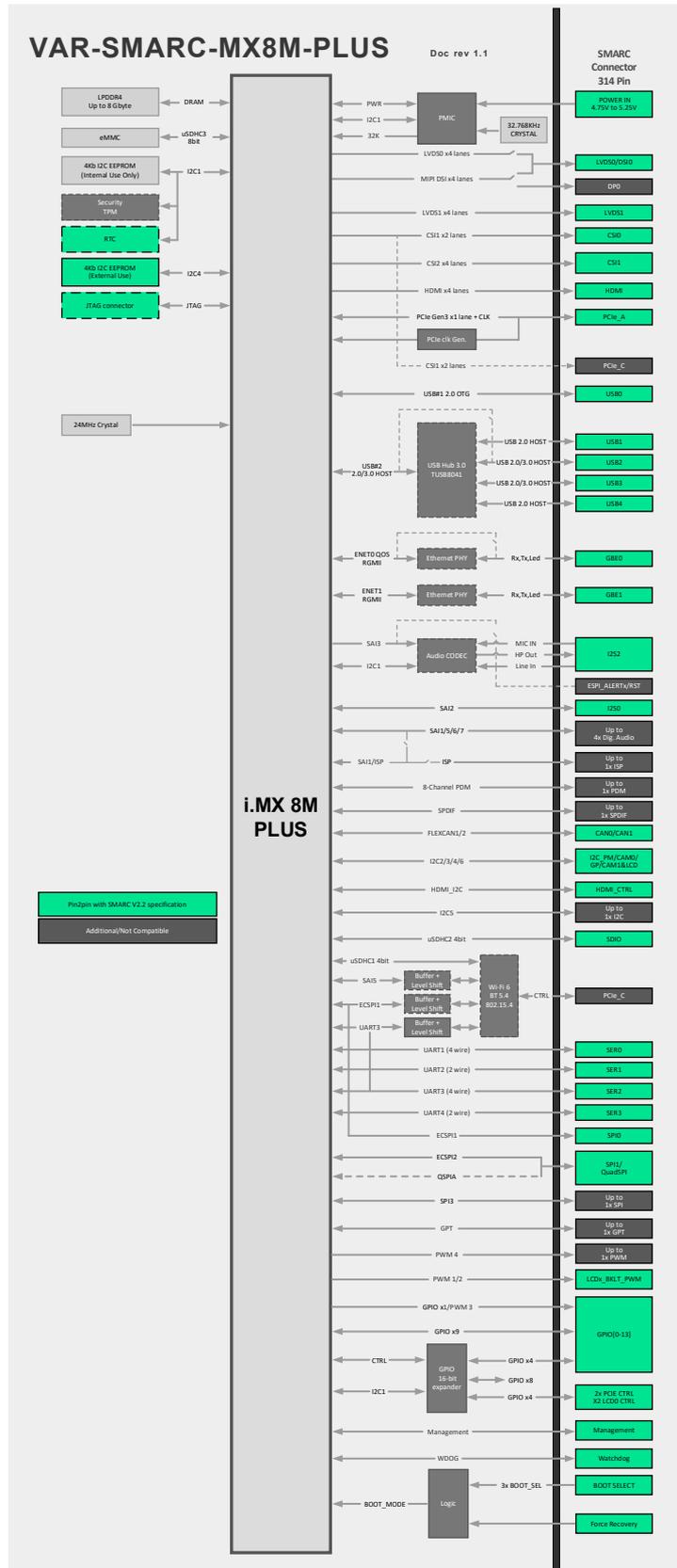
5. Main Hardware Components

This section summarizes the main hardware building blocks of the VAR-SMARC-MX8M-PLUS.

5.1 NXP i.MX 8M Plus

5.1.1 Overview

The i.MX 8M Plus family focuses on machine learning and vision, advanced multimedia, and industrial IoT with high reliability. It is built to meet the needs of Smart Home, Building, City and Industry 4.0 applications.

- Powerful quad or dual Arm® Cortex®-A53 processor with a Neural Processing Unit (NPU) operating at up to 2.3 TOPS.

- Real-time control with Cortex-M7. Robust control networks supported by dual CAN FD (IT version) and dual Gigabit Ethernet, one of which, with Time Sensitive Networking (TSN).

- The multimedia capabilities include video encode (including h.265) and decode, 3D/2D graphic acceleration, and multiple audio and voice functionalities.

- Dual Image Signal Processors and two camera inputs for an effective Vision System.

- High industrial reliability with DRAM inline ECC and ECC on on-chip RAM.

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5.1.2 i.MX 8M Plus Block Diagram
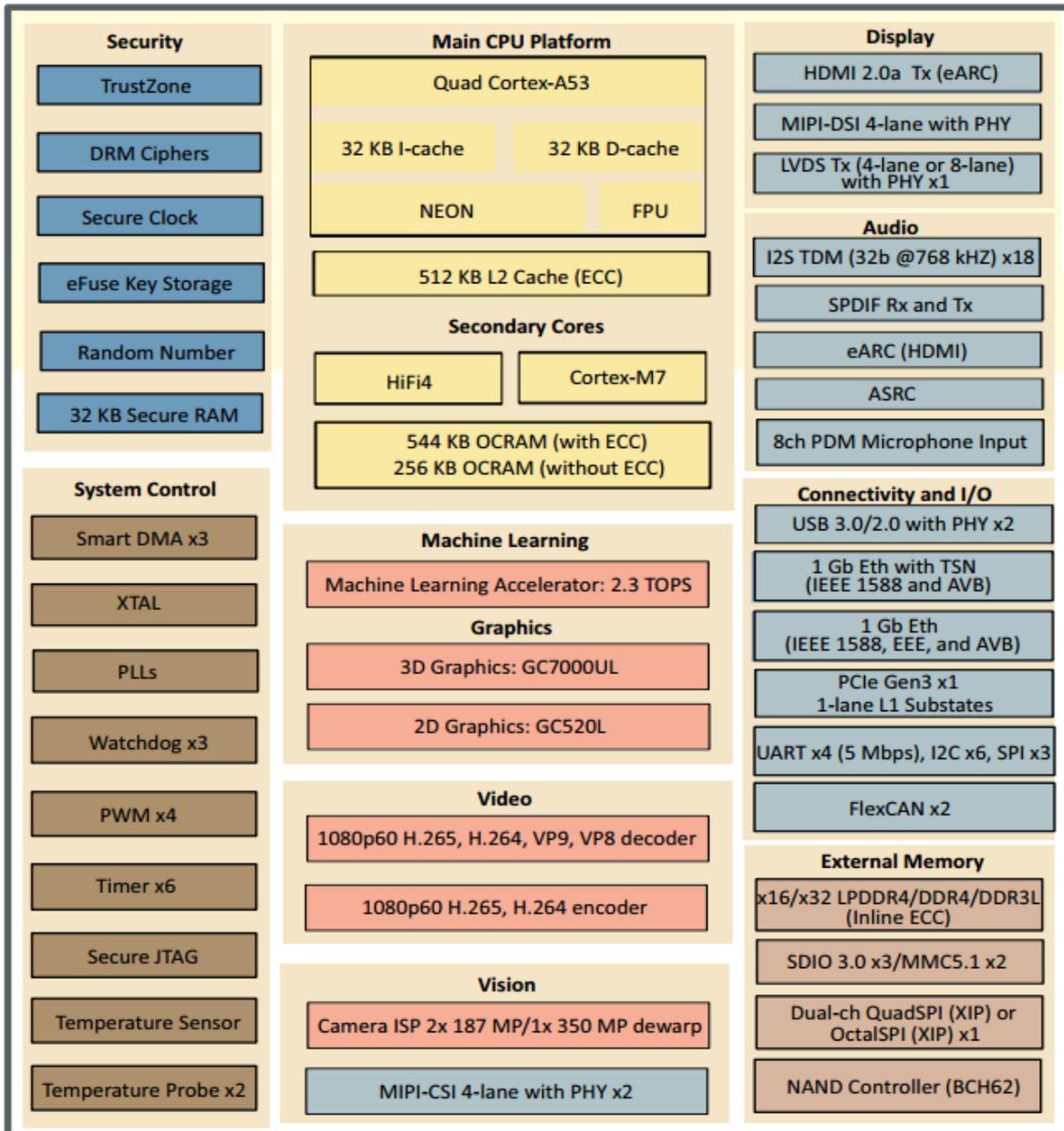
Figure 2 : i.MX 8M Plus Block Diagram

5.1.3 ARM Cortex-A53 MPCore™ Platform

The i.MX 8M Plus family Applications Processors are based on the ARM Cortex-A53 MPCore™ platform, which has the following features:

- Quad symmetric Cortex-A53 processors operation up to 1.8 GHz, including:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - Media Processing Engine (MPE) with NEON technology supporting the Advanced Single Instruction Multiple Data architecture
  - Floating Point Unit (FPU) with support of the VFPv4-D16 architecture
- Support of 64-bit Armv8-A architecture
  512 KB unified L2 cache

5.1.4 Arm Cortex M7 Platform

The Cortex-M7 Core Platform includes the following:

- Low power microcontroller available for customer application:
  - 32 KB L1 Instruction Cache
  - 32 KB L1 Data Cache
  - 256 KB TCM
- Available customer applications include:
  - Low power standby mode
  - IoT device control
  - ML applications

5.1.5 System Bus and Interconnect

System bus and interconnect include the following:

- Network interconnect (NoC) AXI arbiter
- Quality of service controller (QoSC) to configure priorities and limits of AXI transactions
- Performance monitor (PERFMON) to monitor AXI bus activity
- Debug monitor (DBGMON) to record AXI transactions preceding a system reset

5.1.6 Clocking and Resets

Clocking and resets include:

- Clock control module (CCM) provides centralized clock generation and control
  - Simplified clock tree structure
  - Unified clock programming model for each clock root
  - Multicore awareness for resource domains
- System reset controller (SRC) provides reset generation and distribution

5.1.7 Interrupts and DMA

Interrupts and DMA include:

- 160 shared peripheral interrupts routed to Cortex-A53 Global Interrupt Controller GIC) and Cortex-M7 nested vector interrupt controller (NVIC) for flexible interrupt handling
- Three Smart direct memory access (SDMA) engines. Although these three engines
- are identical to each other, they are integrated into the processor to serve different peripherals.
    - SDMA-1 is a general-purpose DMA engine which can be used by low speed peripherals including UART, SPI and also others peripherals.
    - SDMA-2 and SMDA-3 is used for audio interface, including SAI-1/2/3/5/6/7, SPDIF and PDM audio input

5.1.8 On-Chip Memory

The on-chip memory system consists of the following:

- Boot ROM (256KB)
- On-Chip RAM - OCRAM (576KB)
- Audio Processor System RAM - OCRAM_A (256KB)
- On-Chip RAM for State Retention - OCRAM_S (36KB)

5.1.9 External Memory Interface

The external memory interfaces supported on this chip include:

- 32-bit DRAM Interface:
    - LPDDR4-4000
    - DDR4-3200
- 8-bit NAND FLASH, including support for Raw MLC/SLC devices, BCH ECC up to 62-bit, and ONFi3.2 compliance (clock rates up to 100 MHz and data rates up to 200 MB/sec)
- eMMC 5.1 FLASH (2 interfaces)
- SPI NOR FLASH (3 interfaces)
- FlexSPI FLASH with support for XIP (for Cortex-M7 in low-power mode) and support for either one Octal SPI, or parallel read mode of two identical Quad SPI FLASH devices

5.1.10 Timers

- The timers on this chip include:
- One local generic timer integrated into each Cortex-A53 CPU
- Global system counter with timer bus interface to Cortex-A53 MPCore generic timers
- One local system timer (SysTick) integrated into the Cortex-M7 CPU
- Six general purpose timer (GPT) modules
- Three watchdog timer (WDOG) modules
- Four pulse width modulation (PWM) modules

5.1.11 Graphics Processing Unit (GPU)

The chip incorporates the following Graphics Processing Unit (GPU) features:
• One GPU for 2D and composition acceleration

- o   Supports multi-source composition
- o   Supports one-pass filter
- o   Supports tile format

• One GPU for 3D processing

- o   Two Shader Execution Units
- o   Supports OpenGL ES 1.1, 2.0, 3.0, 3.1
- o   Supports OpenCL 3.0
- o   Supports OpenVG 1.1
- o   Supports OpenGL 4.0
- o   Supports EGL 1.5
- o   Supports Vulkan 1.1
- o   Supports tile format

5.1.12 Graphics Processing Unit (VPU)

The chip incorporates the following Video Processing Unit (VPU) features:

- Video Decode:
  - o   1080p60 HEVC/H.265 Main, Main 10 (up to level 5.1) (VPU G2)
  - o   1080p60 VP9 Profile 0, 2 (VPU G2)
  - o   1080p60 VP8 (VPU G1)
  - o   1080p60 AVC/H.264 Baseline, Main, High decoder (VPU G1)
- Video Encode:
  - o   1080p60 AVC/H.264 encoder
  - o   1080p60 HEVC/H.265 encoder
- TrustZone support

5.1.13 Machine Learning: NPU (Neural Processing Unit)

- 2.3 TOP/s Neural Network performance available for user applications
  - o   Speech recognition (e.g., Deep Speech 2)
  - o   Image recognition (e.g., ResNet-50)
  - o   Object detection (e.g., MobileNet-SSD)

5.1.14 Display Interfaces

The chip has the following display support:

- Three LCDIF Display Controllers:
  - One LCDIF drives MIPI DSI
  - One LCDIF drives LVDS Tx
  - One LCDIF drives HDMI Tx
  - Support up to 1920x1200p60 display per LCDIF if no more than 2 instances used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances used simultaneously.
  - Supports 8-bit / 16-bit / 18-bit / 24-bit / 32-bit pixel depth
  - Supports one layer
- MIPI Interface:
  - One 4-lane MIPI DSI interface
  - Two 4-lane MIPI CSI interfaces
- Two 4-lane LVDS interfaces
- ISI (Image Sensor Interface):
  - The ISI is a simple camera interface that supports image processing and transfer via a bus master interface for up to 2 cameras
- Two Camera ISP (Image Signal Processor):
  - When one camera is used, supports up to 12MP@30fps or 4kp45
  - When two cameras are used, each supports up to 1080p80
- HDMI 2.0a
  - HDMI 2.0a Tx supporting one display
    - Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120, 3840 x 2160p30
- Audio support
  - 32 channel audio output support
  - 1 S/PDIF audio eARC input support

5.1.15 Audio

Audio include the following:

- Audio DSP
- S/PDIF Input and Output, including a Raw Capture input mode
- Six external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces, comprising one SAI with 8 TX and 8 RX lanes, one SAI with 4 TX and 4 RX lanes, two SAI with 2 TX and 2 RX lanes, and two SAI with 1 TX and 1 RX lanes.
- PDM Microphone Interface module which supports up to 8-microphones (4 lanes)
- Asynchronous Sample Rate Converter (ASRC) module which supports:
  - Processing of up to 32 audio channels
  - 4 context groups
  - 8 kHz to 384 kHz sample rate
  - 1/16 to 8x sample rate conversion ratio

5.1.16 General Connectivity Interfaces

The chip contains a rich set of general connectivity interfaces, including:

- One PCI Express (PCIe):
    - Single lane supporting PCIe Gen 3
    - Dual mode operation to function as root complex or endpoint
    - Integrated PHY interface
    - Supports L1 low power substate
- Two USB 3.0 Type C controllers with integrated PHY interface
    - Backwards compatibility with USB 2.0
    - Spread spectrum clock support
- Three Ultra Secure Digital Host Controller (uSDHC) interfaces
    - MMC 5.1 compliance with HS400 DDR signaling to support up to 400 MB/sec
    - SD/SDIO 3.01 compliance with 200 MHZ SDR signaling to support up to 100 MB/sec
    - Support for SDXC (extended capacity)
- Two Ethernet controllers, capable of simultaneous operation
    - One Gigabit Ethernet controller with support for EEE, Ethernet AVB and IEEE1588
    - One Gigabit Ethernet controller with support for TSN, EEE, Ethernet AVB and IEEE1588
- Two controller area network (FlexCAN) modules, each optionally supporting flexible data rate (FD)
- Four universal asynchronous receiver/transmitter (UART) modules
- Six I2C modules
- Three SPI modules

5.1.17 Security

Security functions are enabled and accelerated by the following hardware:

- RDC – Resource Domain Controller:
    - Supports 4 domains and up to 8 regions
- Arm TrustZone including the TZ architecture:
    - ARM Cortex-A53 MPCore TrustZone support
- On-chip RAM (OCRAM) secure region protection using OCRAM controller
- High Assurance Boot (HAB)
- Cryptographic Acceleration and Assurance Module (CAAM)
    - Support Widevine and PlayReady content protection
    - Public Key Cryptography (PKHA) with RSA and Elliptic Curve (ECC) algorithms
    - Real-time integrity checker (RTIC)
    - DRM support for RSA, AES, 3DES, DES
    - Side channel attack resistance
    - True random number generation (RNG)
    - Manufacturing protection support
- Secure Non-Volatile Storage (SNVS), including Secure Real Time Clock (SRTC)
- Secure JTAG Controller (SJC)

5.1.18   Multicore Support

Multicore support contains:

- Resource domain controller (RDC) to support isolation and safe sharing of system resources
- Messaging unit (MU)
- Hardware Semaphore (SEMA42)
- Shared bus topology

5.1.19   GPIO and Pin Multiplexing

- General-purpose input/output (GPIO) modules with interrupt capability
- Input/output multiplexing controller (IOMUXC) to provide centralized pad control

5.1.20   Power Management

The power management unit consists of:

- Temperature sensor with programmable trip points
- Flexible power domain partitioning with internal power switches to support efficient power management

5.1.21   System Debug

The system debug features are:

- ARM CoreSight debug and trace architecture
- Embedded Trace FIFO (ETF) with 4 KB internal storage to provide trace buffering
- Unified trace capability for Quad Cortex-A53 and Cortex-M7 CPUs
- Cross Triggering Interface (CTI)
- Support for 5-pin (JTAG) debug interfaces

5.2   Memory

5.2.1   RAM

The VAR-SMARC-MX8M-PLUS is available with up to 8 GB of LPDDR4-4000 memory.

5.2.2   Non-volatile Storage Memory

The VAR-SMARC-MX8M-PLUS is available with a non-volatile MLC eMMC storage memory with optional densities of up to 128GB. It is used for Flash Disk purposes, O.S. run-time-image, Boot-loader and application/user data storage.

5.3   Audio (Optional)

The VAR-SMARC-MX8M-PLUS can be ordered with Cirrus Logic Audio Codec WM8904.
The WM8904 is a high performance ultra-low power stereo CODEC optimized for portable audio applications.
The device features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques. It incorporates an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback.
The ground-referenced headphone output eliminates AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise. Control sequences for audio path setup can be pre-loaded and executed by an integrated control write sequencer to reduce software driver development and minimize pops and clicks via SilentSwitch™ technology. The input impedance is constant with PGA gain setting. A stereo digital microphone interface is provided, with a choice of two inputs. A dynamic range controller provides compression and level control to support a wide range of portable recording applications. Anti-clip and quick release features offer good performance in the presence of loud impulsive noises. ReTuneTM Mobile 5-band parametric equalizer with fully programmable coefficients is integrated for optimization of speaker characteristics. Programmable dynamic range control is also available for maximizing loudness, protecting speakers from clipping and preventing premature shutdown due to battery droop. Common audio sampling frequencies are supported from a wide range of external clocks, either directly or generated via the FLL.

Features:

- 3.0mW quiescent power consumption for DAC to headphone playback
- DAC SNR 96dB typical, THD -86dB typical
- ADC SNR 91dB typical, THD -80dB typical
- 2.4mW quiescent power consumption for analogue bypass playback
- Control write sequencer for pop minimized start-up and shutdown
- Single register writes for default start-up sequence
- Integrated FLL provides all necessary clocks - Self-clocking modes allow processor to sleep - All standard sample rates from 8kHz to 96kHz
- Stereo digital microphone input
- 2 single ended inputs per stereo channel
- Digital Dynamic Range Controller (compressor / limiter)
- Digital sidetone mixing
- Ground-referenced headphone driver

5.4   Wi-Fi + BT + LR-WPAN (Optional)

The module can be ordered with one of the following Wi-Fi modules:

- "WBE":
  Murata Type 2EL - 2.4GHz & 5GHz Wi-Fi® + Bluetooth® 5.4 BR/EDR/LE + 802.15.4 Module based on NXP IW612 chipset
- "WBD":
  Murata Type 2DL -2.4GHz & 5GHz Wi-Fi® + Bluetooth® 5.4 BR/EDR/LE Module based on NXP IW611 chipset
- "WBK":
  Murata Type 2KL - 2.4GHz & 5GHz Wi-Fi™ + Bluetooth® 5.4 Low Energy Module based on NXP IW610F chipset

All realize the necessary PHY/MAC layers to support WLAN applications in conjunction with a host processor over a SDIO interface.
The modules also provide a Bluetooth/BLE platform through the HCI transport layer. Both WLAN and Bluetooth share the same antenna port or may be ordered with dual antenna ports.

5.5   PMIC

The VAR-SMARC-MX8M-PLUS features Dual Freescale/NXP's PCA9450CHN chip as a Power Management Integrated circuit (PMIC) designed specifically for use with NXP's i.MX 8M Plus series of application processors. The PCA9450CHN regulates power rails required on SOM from a single 5V power supply.
The PMIC is fully programmable via the I2C interface and associated register map.
Additional communication is provided by direct logic interfacing including interrupt, watchdog and reset.

5.6   10/100/1000 Mbps Ethernet Transceiver (Optional)

The VAR-SMARC-MX8M-PLUS can be ordered with 2x on board an Integrated Ethernet Transceivers
TI P/N: DP83867IRRGZ.

The DP83867 device is a robust, low power, fully featured Physical Layer transceiver with integrated PMD sublayers to support 10BASE-Te, 100BASETX and 1000BASE-T Ethernet protocols.
The DP83867 is designed for easy implementation of 10/100/1000Mbps Ethernet LANs. DP83867 interfaces directly to twisted pair media via an external transformer. This device interfaces directly to the MAC layer through the IEEE 802.3 Reduced GMII (RGMII).

Key features include:

- Ultra low RGMII latency TX < 90ns, RX < 290ns
- Time Sensitive Network (TSN) compliant
- 16 programmable RGMII delay modes on RX/TX
- Integrated MDI termination resistors
- Programmable RGMII termination impedance
- WoL (Wake-on-LAN) packet detection
- Start of Frame Detect for IEEE 1588 time stamp
- RJ45 mirror mode
- Fully compatible to IEEE 802.3 10BASE-Te, 100BASE-TX, and 1000BASE-T Specification Cable diagnostics

- Fast link drop mode
- Support up to 130m cable length

5.7 USB HUB (optional)

The VAR-SMARC-MX8M-PLUS can be ordered with TI's USB HUB P/N: TUSB8041IRGCR
The TUSB8041 is a four-port USB 3.0 hub. It provides simultaneous SuperSpeed USB and highspeed/full-speed connections on the upstream port and provides SuperSpeed USB, high-speed, fullspeed, or low-speed connections on the downstream ports.

With HUB assembled, the following USB ports are available:
Via SoC:

- 1x USB 2.0 OTG

Via HUB:

- 2x USB 2.0 HOST
- 2x USB 3.0/2.0 HOST

With HUB not assembled, the following USB ports are available:
Via SoC:

- 1x USB 2.0 OTG
- 1x USB 3.0/2.0 HOST

5.8 EEPROM

The SOM uses 4Kbit serial EEPROM to store memory calibration and manufacturing parameters.
This EEPROM is connected to I2C1 bus and intended only for holding the above information.
The SOM may not boot if the contents of EEPROM device are corrupted.

5.9 General Purpose EEPROM

The SOM includes a 4Kbit serial EEPROM which can be used by User for General purposes such as storing Module parameter information, including a Module serial number.
This EEPROM is connected to I2C4 bus.

5.10 Real Time clock (optional)

The VAR-SMARC-MX8M-PLUS includes NXP's Real Time Clock (RTC) IC Clock/Calendar chip P/N: PCF85263ATL/AX.

5.11 TPM (optional)

The VAR-SMARC-MX8M-PLUS can be ordered with a Trusted Platform Module (TPM) 2.0, STMicroelectronics P/N: ST33KTPM2I3WBZB1, or Infineon Technologies P/N: SLB9673XU20FW2613XTMA1.

6. VAR-SMARC-MX8M-PLUS Hardware Configuration

The table below lists the Hardware configurations options orderable for the VAR-SMARC-MX8M-PLUS.

Table 1 Hardware Configuration Options

Option	Description
EC1	Ethernet PHY1 assembled on SOM for exporting GBE0 I/F
EC2	Ethernet PHY2 assembled on SOM for exporting GBE1 I/F
AC	Audio Codec assembled on SOM
WBE	2.4GHz & 5GHz Wi-Fi® + Bluetooth® + 802.15.4 Module assembled on SOM (Murata 2EL)
WBD	2.4GHz & 5GHz Wi-Fi® + Bluetooth® Module assembled on SOM (Murata 2DL)
WBK	2.4GHz & 5GHz Wi-Fi™ + Bluetooth® 5.4 Low Energy Module (Murata 2KL)
HUB	USB HUB assembled on SOM
DSI2LV	DSI lanes are exported to SMARC connector pins instead of LVDS0 lanes. By default, DSI is exported on SMARC DP0 pins. In DSI2LV assembly, DSI will not be exported on DP0 pins but will be exported instead on LVDS0 pins
RTC	Internal RTC chip assembled on SOM
TPMST/TPMIF	TPMST: Internal ST TPM secure chip assembled on SOM TPMIF: Internal Infineon secure chip assembled on SOM
BTPCM	In WBD/WBE/WBK: SAI5 balls internally connected to Bluetooth PCM lines [1]
COEX	In WBD/WBE/WBK and no CSI0: Expose WCI-2 coexistence management lines [1]
BTRST	In WBD/WBE/WBK and no CSI0: Expose Bluetooth® and 802.15.4 reset lines [1]
WRST	In WBD/WBEL/WBK: Expose 2.4GHz & 5GHz Wi-Fi® reset line [1]
WAKE	In WBD/WBE/WBK: Expose Wi-Fi/ BT wakeup lines [1]
ANT2	In WBD/WBE/WBK: Dual antenna mode. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4 [1]
QSPI	QSPI I/F signals exported to SMARC ESPI pins instead of SPI1
SAI3	In no AC: Additional SAI3 I/F signals exported to SMARC connector pins
CHG	Optional route of SMARC GPIOs to SMARC Charger pins
ETH_INT	In EC1/EC2 configuration, expose Ethernet PHYs interrupt lines
SPI BOOT	Boot buffer to support boot from SPI assembled on SOM [1]

NOTE
[1] This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

Note: Other orderable options are available and are not part of this datasheet.
Please refer to Variscite official website for a full list of configuration options.

7. External Connectors

7.1 Board to Board Connector

The VAR-SMARC-MX8M-PLUS exposes 314 edge fingers that mate with a low profile 314 pin 0.5mm pitch right angle connector

The recommended mating connectors for Carrier interfacing are the connectors commonly used for MXM3 graphics cards. Recommended Carrier connectors from SMARC 2.2 specification section 5.1 "Carrier Connector" are:

Vendor	Vendor P/N	Stack Height	Body Height	Contact Plating
Foxconn	AS0B821-S43B - 7H	1.5mm	4.3mm	Flash
Foxconn	AS0B826-S43B - 7H	1.5mm	4.3mm	10 u-in
JAE	MM70-314B2-1-R500	1.5mm	4.3mm	0.1 u-meter
Aces	91781-314 2 8-001	2.7mm	5.2mm	3 u-in
Foxconn	AS0B821-S55B - 7H	2.7mm	5.5mm	Flash
Foxconn	AS0B826-S55B - 7H	2.7mm	5.5mm	10 u-in
JAE	MM70-314B1-2-R300	4.4mm	6.7mm	0.3 u-meter
Aces	91781-314 0 M-001	5.0mm	7.5mm	3 u-in
Amphenol	10151114-001TLF	5.0mm	7.8mm	30 u-in
Foxconn	AS0B821-S78B - 7H	5.0mm	7.8mm	Flash
Foxconn	AS0B826-S78B - 7H	5.0mm	7.8mm	10 u-in
Yamaichi	CN113-314-2001-VE-TR	5.0mm	7.8mm	0.3 u-meter

Notes:

- Please check the datasheet of the connectors for specifics and possible deviations
- The SMARC Module uses the connector in a way quite different from the MXM3 usage
  Many of the vendor drawings for the connectors listed above show a PCB footprint pattern for use with an MXM3 graphics card. This footprint, and the associated pin numbering, is not suitable for SMARC use. The MXM3 standard gangs large groups of pins together to provide ~80W capable power paths needed for X86 graphics cards. The SMARC Module "ungangs" these pins to allow more signal pins. Footprint and pin numbering information for application of this 314 pin connector to SMARC is given in SMARC 2.2 specification section 5.

7.2 Wi-Fi & BT Connector

- Modules with Wi-Fi *"WBE", "WBD", "WBK" Configuration -* a combined Wi-Fi + BT antenna connector is assembled.
- In case of Modules with Wi-Fi *"WBE", "WBD", "WBK" Configuration & "ANT2" Configuration -* dual Antenna connectors are assembled.
- Connector type: U.FL JACK connector
- Cable and antenna shall have a 50 Ohm characteristic impedance

7.3 JTAG Header

In addition to the 200-pin SO-DIMM interface, the SOM exposes the JTAG interface via an optional Connector JST P/N: SM10B-SRSS-TB. Recommended mating connector is JST P/N: 10SR-3S.

7.4 VAR-SMARC-MX8M-PLUS Connector Pin-out

Table 2: VAR-SMARC-MX8M-PLUS SMARC connector Pinout

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P1		SMB_ALERT#	SAI1_TXD7(GPIO4_IO19)		1.8V; PU 2.2K	SOC.AJ13
P2		GND	GND	Digital Ground;		GND
P3		CSI1_CK+	MIPI_CSI2_CLK_P			SOC.A23
P4		CSI1_CK-	MIPI_CSI2_CLK_N			SOC.B23
P5		GBE1_SDP	SAI1_RXC(ENET1_1588_EVENT0_OUT)_3V3	GBE1 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.AH8 (via push pull level shifter)
P6		GBE0_SDP	GPIO1_IO09(ENET_QOS_1588_EVENT0_ OUT)_3V3	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)
P7		CSI1_RX0+	MIPI_CSI2_D0_P			SOC.A25
P8		CSI1_RX0-	MIPI_CSI2_D0_N			SOC.B25
P9		GND	GND	Digital Ground;		GND
P10		CSI1_RX1+	MIPI_CSI2_D1_P			SOC.A24
P11		CSI1_RX1-	MIPI_CSI2_D1_N			SOC.B24
P12		GND	GND	Digital Ground;		GND
P13		CSI1_RX2+	MIPI_CSI2_D2_P			SOC.A22
P14		CSI1_RX2-	MIPI_CSI2_D2_N			SOC.B22
P15		GND	GND	Digital Ground;		GND
P16		CSI1_RX3+	MIPI_CSI2_D3_P			SOC.A21
P17		CSI1_RX3-	MIPI_CSI2_D3_N			SOC.B21
P18		GND	GND	Digital Ground;		GND
P19	no EC1	GBE0_MDI3-	ENET_QOS_RGMII_RD3	Available in SOM without "EC1" configuration;	1.8V	SOC.AF28
P19	EC1	GBE0_MDI3-	ETH0_MDI_D_M	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.11

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P20	no EC1	GBE0_MDI3+	ENET_QOS_RGMII_RD2	Available in SOM without "EC1" configuration;	1.8V	SOC.AF29
P20	EC1	GBE0_MDI3+	ETH0_MDI_D_P	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.10
P21	no EC1	GBE0_LINK_MID#	ENET_QOS_RGMII_TXC	Available in SOM without "EC1" configuration;	1.8V	SOC.AE24
P21	EC1	GBE0_LINK_MID#	ETH0_LED_LINK_100	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.39 (Via inv. FET)
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC	Available in SOM without "EC1" configuration;	1.8V	SOC.AE29
P22	EC1	GBE0_LINK_MAX#	ETH0_LED_LINK_1000	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.46 (Via inv. FET)
P23	no EC1	GBE0_MDI2-	ENET_QOS_RGMII_RD1	Available in SOM without "EC1" configuration;	1.8V	SOC.AG28
P23	EC1	GBE0_MDI2-	ETH0_MDI_C_M	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.8
P24	no EC1	GBE0_MDI2+	ENET_QOS_RGMII_RD0	Available in SOM without "EC1" configuration;	1.8V	SOC.AG29
P24	EC1	GBE0_MDI2+	ETH0_MDI_C_P	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.7
P25	no EC1	GBE0_LINK_ACT#	ENET_QOS_RGMII_RX_CTL	Available in SOM without "EC1" configuration;	1.8V	SOC.AE28
P25	EC1	GBE0_LINK_ACT#	ETH0_LED_ACT	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.45 (Via inv. FET)
P26	no EC1	GBE0_MDI1-	ENET_QOS_RGMII_TD0	Available in SOM without "EC1" configuration;	1.8V	SOC.AC25
P26	EC1	GBE0_MDI1-	ETH0_MDI_B_M	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.5
P27	no EC1	GBE0_MDI1+	ENET_QOS_RGMII_TD1	Available in SOM without "EC1" configuration;	1.8V	SOC.AE26
P27	EC1	GBE0_MDI1+	ETH0_MDI_B_P	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.4
P28	no ETH_INT	GBE0_CTREF	NC	In "no ETH_INT" configuration this pin is Not Connected;		NC
P28	EC1 & ETH_INT	GBE0_CTREF	ETH0_INT_IN	Signal source is Ethernet PHY EC1;	1.8V	GBE0_DP83867IRRGZ.44
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P29	EC1	GBE0_MDI0-	ETH0_MDI_A_M	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.2
P30	no EC1	GBE0_MDI0+	ENET_QOS_RGMII_TD3	Available in SOM without "EC1" configuration;	1.8V	SOC.AD24
P30	EC1	GBE0_MDI0+	ETH0_MDI_A_P	Signal source is Ethernet PHY EC1;		GBE0_DP83867IRRGZ.1
P31		SPI0_CS1#	SAI1_MCLK(GPIO4_IO20)		1.8V	SOC.AE12
P32		GND	GND	Digital Ground;		GND

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P33		SDIO_WP	SD2_WP(USDHC2_WP)		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AC26
P34		SDIO_CMD	SD2_CMD(USDHC2_CMD)		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AB28
P35		SDIO_CD#	SD2_CD_B(USDHC2_CD_B)		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AD29
P36		SDIO_CK	SD2_CLK(USDHC2_CLK)		Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
P37		SDIO_PWR_EN	GPIO1_IO08_3V3	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P38		GND	GND	Digital Ground;		GND
P39		SDIO_D0	SD2_DATA0(USDHC2_DATA0)		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
P40		SDIO_D1	SD2_DATA1(USDHC2_DATA1)		Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
P41		SDIO_D2	SD2_DATA2(USDHC2_DATA2)		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
P42		SDIO_D3	SD2_DATA3(USDHC2_DATA3)		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
P43	no WBE	SPI0_CS0#	I2C2_SDA(ECSPI1_SS0)	Available in SOM without "WBE" configuration;	1.8V	SOC.AE8
P43	WBE	SPI0_CS0#	GPIO1_IO00	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
P44		SPI0_CK	I2C1_SCL(ECSPI1_SCLK0)		1.8V	SOC.AC8
P45		SPI0_DIN	I2C2_SCL(ECSPI1_MISO)		1.8V	SOC.AH6
P46		SPI0_DO	I2C1_SDA(ECSPI1_MOSI)		1.8V	SOC.AH7
P47		GND	GND	Digital Ground;		GND
P48		SATA_TX+	NC			NC
P49		SATA_TX-	NC			NC
P50	no AC	GND	GND	Available in SOM without "AC" configuration;		GND
P50	AC	GND	AGND	Signal source is Audio Codec;		AGND

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P51		SATA_RX+	NC			NC
P52		SATA_RX-	NC			NC
P53		GND	GND	Digital Ground;		GND
P53		GND	GND	Digital Ground;		GND
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(QSPI_A_SS0_B)	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(GPIO3_IO14)_QSPI_A_DQS		1.8V	SOC.R26
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(QSPI_A_SCLK)	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(QSPI_A_DATA1)	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(QSPI_A_DATA0)	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
P59		GND	GND	Digital Ground;		GND
P60		USB0+	USB1_DP	Soc USB1 - USB0 2.0 - OTG;		SOC.D10
P61		USB0-	USB1_DN	Soc USB1 - USB0 2.0 - OTG;		SOC.E10
P62		USB0_EN_OC#	GPIO1_IO13_3V3	SoC USB1 - USB0 Over-Current Sense GPIO;	3.3V, via bidirectional OD level shifter; with 10K PU	SOC.A6 (via bidirectional OD level shifter)
P63		USB0_VBUS_DET	USB1_VBUS	Soc USB1 - USB0 VBUS;	5V	SOC.A11
P64		USB0_OTG_ID	GPIO1_IO10(GPIO1_IO10)_3V3	SoC USB1 - USB0_OTG_ID GPIO;	3.3V, Input via push pull level shifter	SOC.B7 (via push pull level shifter)
P65	no HUB	USB1+	NC	In "no HUB" configuration this pin is Not Connected;		NC
P65	HUB	USB1+	USBH_P1_DP	Available in SOM with "HUB" configuration; USB1 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.1

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P66	no HUB	USB1-	NC	In "no HUB" configuration this pin is Not Connected;		NC
P66	HUB	USB1-	USBH_P1_DN	Available in SOM with "HUB" configuration; USB1 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.2
P67	no HUB	USB1_EN_OC#	NC	In "no HUB" configuration this pin is Not Connected;		NC
P67	HUB	USB1_EN_OC#	P1_EN_OC_N_3V3	Available in SOM with "HUB" configuration; USB1 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041IRGCR.46
P68		GND	GND	Digital Ground;		GND
P69	no HUB	USB2+	USB2_D_P	Available in SOM without "HUB" configuration; SoC USB2 2.0 signal;		SOC.D14
P69	HUB	USB2+	USBH_P2_DP	Available in SOM with "HUB" configuration; USB2 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.9
P70	no HUB	USB2-	USB2_D_N	Available in SOM without "HUB" configuration; SoC USB2 2.0 signal		SOC.E14
P70	HUB	USB2-	USBH_P2_DN	Available in SOM with "HUB" configuration; USB2 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.10
P71	no HUB	USB2_EN_OC#	GPIO_EXP_P1_2__P2_EN_OC_N_3V3	Available in SOM without "HUB configuration; USB2 Enable/Over-Current Sense; Signal source is GPIO Expander P1_2;	3.3V via bidirectional OD level shifter with 10K PU	PCAL6416AHF,128.12 (via bidirectional OD level shifter)
P71	HUB	USB2_EN_OC#	P2_EN_OC_N_3V3	Available in SOM with "HUB" configuration; USB2 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041IRGCR.47
P72		RSVD	NC			NC
P73		RSVD	NC			NC
P74	no HUB	USB3_EN_OC#	NC	In "no HUB" configuration this pin is Not Connected;		NC
P74	HUB	USB3_EN_OC#	P3_EN_OC_N_3V3	Available in SOM with "HUB" configuration; USB3 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041IRGCR.44
P75		PCIE_A_RST#	GPIO_EXP_P1_6__PCIE_A_RST#_3V3	Signal source is GPIO Expander P1_6;	3.3V, via bidirectional OD level shifter; with 10k PU	PCAL6416AHF,128.16 (via bidirectional OD level shifter)
P76	no HUB	USB4_EN_OC#	NC	In "no HUB" configuration this pin is Not Connected;		NC
P76	HUB	USB4_EN_OC#	P4_EN_OC_N_3V3	Available in SOM with "HUB" configuration; USB4 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041IRGCR.43

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P77		PCIE_B_CKREQ#	NC			NC
P78		PCIE_A_CKREQ#	PCIE_A_CKREQ#	Input signal to on SOM clock generator;	3.3V; PU 20K	DSC557-0344FL1T.1 (Via inv. FET)
P79		GND	GND	Digital Ground;		GND
P80	no COEX & no BTRST	PCIE_C_REFCK+	MIPI_CSI1_D2_P	Available in SOM without "COEX" and without "BTRST" configuration;		SOC.D24
P80	COEX	PCIE_C_REFCK+	COEX_SIN_1V8	Available in SOM with "COEX" configuration;	1.8V	LBES5PL2xL.69
P80	no COEX & BTRST	PCIE_C_REFCK+	NC	In "no COEX and BTRST" configuration this pin is Not Connected;		NC
P81	no COEX & no BTRST	PCIE_C_REFCK-	MIPI_CSI1_D2_N	Available in SOM without "COEX" and without "BTRST" configuration;		SOC.E24
P81	COEX	PCIE_C_REFCK-	COEX_SOUT_1V8	Available in SOM with "COEX" configuration;	1.8V	LBES5PL2xL.70
P81	no COEX & BTRST	PCIE_C_REFCK-	NC	In "no COEX and BTRST" configuration this pin is Not Connected;		NC
P82		GND	GND	Digital Ground;		GND
P83		PCIE_A_REFCK+	PCIE_A_REFCK+	Signal Source is on SOM clock generator;		DSC557-0344FL1T.8
P84		PCIE_A_REFCK-	PCIE_A_REFCK-	Signal Source is on SOM clock generator;		DSC557-0344FL1T.9
P85		GND	GND	Digital Ground;		GND
P86		PCIE_A_RX+	PCIE_RXN_P			SOC.A14
P87		PCIE_A_RX-	PCIE_RXN_N			SOC.B14
P88		GND	GND	Digital Ground;		GND
P89		PCIE_A_TX+	PCIE_TXN_P			SOC.A15
P90		PCIE_A_TX-	PCIE_TXN_N			SOC.B15
P91		GND	GND	Digital Ground;		GND
P92		HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P			SOC.AH27
P93		HDMI_D2- / DP1_LANE0-	HDMI_TX2_N			SOC.AJ27
P94		GND	GND	Digital Ground;		GND
P95		HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P			SOC.AH26
P96		HDMI_D1- / DP1_LANE1-	HDMI_TX1_N			SOC.AJ26
P97		GND	GND	Digital Ground;		GND
P98		HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P			SOC.AH25

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P99		HDMI_D0- / DP1_LANE2-	HDMI_TX0_N			SOC.AJ25
P100		GND	GND	Digital Ground;		GND
P101		HDMI_CK+ / DP1_LANE3+	HDMI_TXC_P			SOC.AH24
P102		HDMI_CK- / DP1_LANE3-	HDMI_TXC_N			SOC.AJ24
P103		GND	GND	Digital Ground;		GND
P104		HDMI_HPD / DP1_HPD	HDMI_HPD		1.8V	SOC.AE22
P105		HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL(HDMI_SCL)		1.8V	SOC.AC22
P106		HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA(HDMI_SDA)		1.8V	SOC.AF22
P107		DP1_AUX_SEL	NC			NC
P108		GPIO0 / CAM0_PWR#	GPIO_EXP_P0_0__GPIO0_CAM0_PWR#	Signal source is GPIO Expander P0_0;	1.8V	PCAL6416AHF,128.1
P109		GPIO1 / CAM1_PWR#	GPIO_EXP_P0_1__GPIO1_CAM1_PWR#	Signal source is GPIO Expander P0_1;	1.8V	PCAL6416AHF,128.2
P110		GPIO2 / CAM0_RST#	GPIO_EXP_P0_2__GPIO2_CAM0_RST#	Signal source is GPIO Expander P0_2;	1.8V	PCAL6416AHF,128.3
P111		GPIO3 / CAM1_RST#	GPIO_EXP_P0_3__GPIO3_CAM1_RST#	Signal source is GPIO Expander P0_3;	1.8V	PCAL6416AHF,128.4
P112		GPIO4 / HDA_RST#	GPIO1_IO03		1.8V	SOC.D6
P113		GPIO5 / PWM_OUT	GPIO1_IO14(PWM3_OUT)		1.8V	SOC.A4
P114		GPIO6 / TACHIN	GPIO1_IO05		1.8V	SOC.B4
P115		GPIO7	GPIO1_IO00	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
P116		GPIO8	SAI1_RXD0(GPIO4_IO02)		1.8V	SOC.AC10
P117		GPIO9	GPIO1_IO01		1.8V	SOC.E8
P118		GPIO10	GPIO1_IO07		1.8V	SOC.F6
P119		GPIO11	GPIO1_IO06	In SOM with "CHG" configuration, Duplicate pin on S156;	1.8V	SOC.A3
P120		GND	GND	Digital Ground;		GND
P121		I2C_PM_CK	SD1_DATA6(I2C2_SCL)		1.8V; PU 2.2K	SOC.AA28
P122		I2C_PM_DAT	SD1_DATA7(I2C2_SDA)		1.8V; PU 2.2K	SOC.U25
P123		BOOT_SEL0#	BOOT_SEL0#	boot select signal, implemented with internal logic;	1.8V; PU 10K	
P124		BOOT_SEL1#	BOOT_SEL1#	boot select signal, implemented with internal logic;	1.8V; PU 10K	
P125		BOOT_SEL2#	BOOT_SEL2#	boot select signal, implemented with internal logic;	1.8V; PU 10K	

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P126		RESET_OUT#	POR_B		1.8V; PU 10K	SOC.J29
P127		RESET_IN#	PMIC_RST_B	SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset.	1.8V, Input via diode; PU 10K	PCA9450CHNY.8 via diode; J1.8
P128		POWER_BTN#	ONOFF		1.8V; PU 10K	SOC.G22
P129		SER0_TX	UART1_TXD(UART1_TX)		1.8V	SOC.AJ3
P130		SER0_RX	UART1_RXD(UART1_RX)		1.8V; PU 100K	SOC.AD6
P131		SER0_RTS#	UART3_RXD(UART1_CTS)		1.8V	SOC.AE6
P132		SER0_CTS#	UART3_TXD(UART1_RTS)		1.8V; PU 100K	SOC.AJ4
P133		GND	GND	Digital Ground;		GND
P134		SER1_TX	UART2_TXD(UART2_TX)	Used as debug UART on Variscite base board	1.8V	SOC.AH4
P135		SER1_RX	UART2_RXD(UART2_RX)	Used as debug UART on Variscite base board	1.8V; PU 100K	SOC.AF6
P136		SER2_TX	ECSPI1_MOSI(UART3_TX)	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P137		SER2_RX	ECSPI1_SCLK(UART3_RX)	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AF20
P138		SER2_RTS#	ECSPI1_MISO(UART3_CTS)	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P139		SER2_CTS#	ECSPI1_SS0(UART3_RTS)	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20
P140		SER3_TX	UART4_TXD(UART4_TX)		1.8V	SOC.AH5
P141		SER3_RX	UART4_RXD(UART4_RX)		1.8V; PU 100K	SOC.AJ5
P142		GND	GND	Digital Ground;		GND
P143		CAN0_TX	SPDIF_TX(FLEXCAN1_TX)		1.8V	SOC.AE18
P144		CAN0_RX	SPDIF_RX(FLEXCAN1_RX)		1.8V	SOC.AD18
P145		CAN1_TX	HDMI_CEC(FLEXCAN2_TX)		1.8V	SOC.AD22

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
P146		CAN1_RX	SAI5_MCLK(CAN2_RX)		1.8V	SOC.AF14
P147		VDD_IN	VDD_IN	SOM Power;		VDD_IN
P148		VDD_IN	VDD_IN	SOM Power;		VDD_IN
P149		VDD_IN	VDD_IN	SOM Power;		VDD_IN
P150		VDD_IN	VDD_IN	SOM Power;		VDD_IN
P151		VDD_IN	VDD_IN	SOM Power;		VCC_SOM
P152		VDD_IN	VDD_IN	SOM Power;		VCC_SOM
P153		VDD_IN	VDD_IN	SOM Power;		VCC_SOM
P154		VDD_IN	VBAT	SOM Power;		VDD_IN
P155		VDD_IN	VBAT	SOM Power;		VDD_IN
P156		VDD_IN	VBAT	SOM Power;		VDD_IN
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(I2C6_SCL)	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(I2C6_SDA)	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S3		GND	GND	Digital Ground;		GND
S4		RSVD	NC			NC
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(I2C3_SCL)		1.8V; PU 2.2K	SOC.AJ7
S6		CAM_MCK	GPIO1_IO15(CCM_CLKO2)		1.8V	SOC.B5
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(I2C3_SDA)		1.8V; PU 2.2K	SOC.AJ6
S8		CSI0_CK+	MIPI_CSI1_CLK_P			SOC.D22
S9		CSI0_CK-	MIPI_CSI1_CLK_N			SOC.E22
S10		GND	GND	Digital Ground;		GND
S11		CSI0_RX0+	MIPI_CSI1_D0_P			SOC.D18
S12		CSI0_RX0-	MIPI_CSI1_D0_N			SOC.E18
S13		GND	GND	Digital Ground;		GND
S14		CSI0_RX1+	MIPI_CSI1_D1_P			SOC.D20
S15		CSI0_RX1-	MIPI_CSI1_D1_N			SOC.E20
S16		GND	GND	Digital Ground;		GND
S17	no EC2	GBE1_MDI0+	NC	In "no EC2" configuration this pin is Not connected;		NC

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S17	EC2	GBE1_MDI0+	ETH1_MDI_A_P	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.1
S18	no EC2	GBE1_MDI0-	NC	In "no EC2" configuration this pin is Not connected;		NC
S18	EC2	GBE1_MDI0-	ETH1_MDI_A_M	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.2
S19	no EC2	GBE1_LINK_MID#	NC	In "no EC2" configuration this pin is Not connected;		NC
S19	EC2	GBE1_LINK_MID#	ETH1_LED_LINK_100	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP83867IRRGZ.39 (Via inv. FET)
S20	no EC2	GBE1_MDI1+	NC	In "no EC2" configuration this pin is Not connected;		NC
S20	EC2	GBE1_MDI1+	ETH1_MDI_B_P	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.4
S21	no EC2	GBE1_MDI1-	NC	In "no EC2" configuration this pin is Not connected;		NC
S21	EC2	GBE1_MDI1-	ETH1_MDI_B_M	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.5
S22	no EC2	GBE1_LINK_MAX#	NC	In "no EC2" configuration this pin is Not connected;		NC
S22	EC2	GBE1_LINK_MAX#	ETH1_LED_LINK_1000	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP83867IRRGZ.46 (Via inv. FET)
S23	no EC2	GBE1_MDI2+	NC	In "no EC2" configuration this pin is Not connected;		NC
S23	EC2	GBE1_MDI2+	ETH1_MDI_C_P	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.7
S24	no EC2	GBE1_MDI2-	NC	In "no EC2" configuration this pin is Not connected;		NC
S24	EC2	GBE1_MDI2-	ETH1_MDI_C_M	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.8
S25		GND	GND	Digital Ground;		GND
S26	no EC2	GBE1_MDI3+	NC	In "no EC2" configuration this pin is Not connected;		NC
S26	EC2	GBE1_MDI3+	ETH1_MDI_D_P	Signal source is Ethernet PHY EC2;	1.8V	GBE1_DP83867IRRGZ.10
S27	no EC2	GBE1_MDI3-	NC	In "no EC2" configuration this pin is Not connected;		NC
S27	EC2	GBE1_MDI3-	ETH1_MDI_D_M	Signal source is Ethernet PHY EC2;		GBE1_DP83867IRRGZ.11
S28	no ETH_INT	GBE1_CTREF	NC	In "no ETH_INT" configuration this pin is Not Connected;		NC
S28	EC2 & ETH_INT	GBE1_CTREF	ETH1_INT_IN	Signal source is Ethernet PHY EC2;	1.8V	GBE1_DP83867IRRGZ.44
S29		PCIE_D_TX+ / SERDES_0_TX+	NC			NC
S30		PCIE_D_TX- / SERDES_0_TX-	NC			NC
S31	no EC2	GBE1_LINK_ACT#	NC	In "no EC2" configuration this pin is Not connected;		NC
S31	EC2	GBE1_LINK_ACT#	ETH1_LED_ACT	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP83867IRRGZ.45 (Via inv. FET)

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S32		PCIE_D_RX+ / SERDES_0_RX+	NC			NC
S33		PCIE_D_RX- / SERDES_0_RX-	NC			NC
S34		GND	GND	Digital Ground;		GND
S35	no HUB	USB4+	NC	In "no HUB" configuration this pin is Not Connected;		NC
S35	HUB	USB4+	USBH_P4_DP	Available in SOM with "HUB" configuration; USB4 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.24
S36	no HUB	USB4-	NC	In "no HUB" configuration this pin is Not Connected;		NC
S36	HUB	USB4-	USBH_P4_DN	Available in SOM with "HUB" configuration; USB4 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.25
S37		USB3_VBUS_DET	NC			NC
S38		AUDIO_MCK	SAI2_MCLK(SAI2_MCLK)		1.8V	SOC.AJ15
S39		I2S0_LRCK	SAI2_TXFS(SAI2_TX_SYNC)		1.8V	SOC.AJ17
S40		I2S0_SDOUT	SAI2_TXD(SAI2_TX_DATA0)		1.8V	SOC.AH16
S41		I2S0_SDIN	SAI2_RXD(SAI2_RX_DATA0)		1.8V	SOC.AJ14
S42		I2S0_CK	SAI2_TXC(SAI2_TX_BCLK)		1.8V	SOC.AH15
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SAI3_RX_SYNC)	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S43	AC	ESPI_ALERT0#	DMIC_CLK	Signal source is Audio Codec;	1.8V	WM8904.1
S43	no AC & no SAI3	ESPI_ALERT0#	NC			NC
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(SAI3_RX_BCLK)	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
S44	AC	ESPI_ALERT1#	DMIC_DATA	Signal source is Audio Codec;	1.8V	WM8904.27
S44	no AC & no SAI3	ESPI_ALERT1#	NC			NC
S45		MDIO_CLK	ENET_QOS_MDC	GBE1/2 MDIO Clock Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V	SOC.AH28
S46		MDIO_DAT	ENET_QOS_MDIO	GBE1/2 MDIO Data Signal; Pin alternate function cannot be changed when	1.8V; PU 1.47K	SOC.AH29

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
				using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration		
S47		GND	GND	Digital Ground;		GND
S48		I2C_GP_CK	I2C4_SCL	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
S49		I2C_GP_DAT	I2C4_SDA	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(SAI3_TX_SYNC)	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S50	AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	LINEIN1_RP	Signal source is Audio Codec;		WM8904.24
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SAI3_TX_DATA0)	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
S51	AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	LINEIN1_LP	Signal source is Audio Codec;		WM8904.26
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(SAI3_RX_DATA0)	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S52	AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	HPLOUT	Signal source is Audio Codec;		WM8904.13
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(SAI3_TX_BCLK)	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
S53	AC	I2S2_CK / HDA_CK / SNDW_CLK0	HPROUT	Signal source is Audio Codec;		WM8904.15
S54	no EC1	SATA_ACT#	ENET_QOS_RGMII_TX_CTL	Available in SOM without "EC1" configuration;	1.8V	SOC.AH13
S54	EC1	SATA_ACT#	NC	In "EC1" configuration this pin is Not Connected;		NC
S55		USB5_EN_OC#	NC			NC
S56	no QSPI	ESPI_IO_2 / QSPI_IO_2	NC	In "no QSPI" configuration this pin is Not Connected;		NC
S56	QSPI	ESPI_IO_2 / QSPI_IO_2	NAND_DATA02(QSPI_A_DATA2)	Available in SOM with "QSPI" configuration;	1.8V	SOC.L24
S57	no QSPI	ESPI_IO_3 / QSPI_IO_3	NC	In "no QSPI" configuration this pin is Not Connected;		NC
S57	QSPI	ESPI_IO_3 / QSPI_IO_3	NAND_DATA03(QSPI_A_DATA3)	Available in SOM with "QSPI" configuration;	1.8V	SOC.N24
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
S58	AC	ESPI_RESET#	HPOUTFB	Signal source is Audio Codec;		WM8904.14

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S58	no AC & no SAI3	ESPI_RESET#	NC			NC
S59		USB5+	NC			NC
S60		USB5-	NC			NC
S61		GND	GND	Digital Ground;		GND
S62	no HUB	USB3_SSTX+	NC	In "no HUB" configuration this pin is Not Connected;		NC
S62	HUB	USB3_SSTX+	USBH_P3_C_SSTXP	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.19
S63	no HUB	USB3_SSTX-	NC	In "no HUB" configuration this pin is Not Connected;		NC
S63	HUB	USB3_SSTX-	USBH_P3_C_SSTXN	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.20
S64		GND	GND	Digital Ground;		GND
S65	no HUB	USB3_SSRX+	NC	In "no HUB" configuration this pin is Not Connected;		NC
S65	HUB	USB3_SSRX+	USBH_P3_SSRXP	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.22
S66	no HUB	USB3_SSRX-	NC	In "no HUB" configuration this pin is Not Connected;		NC
S66	HUB	USB3_SSRX-	USBH_P3_SSRXN	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.23
S67		GND	GND	Digital Ground;		GND
S68	no HUB	USB3+	NC	In "no HUB" configuration this pin is Not Connected;		NC
S68	HUB	USB3+	USBH_P3_DP	Available in SOM with "HUB" configuration; USB3 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.17
S69	no HUB	USB3-	NC	In "no HUB" configuration this pin is Not Connected;		NC
S69	HUB	USB3-	USBH_P3_DN	Available in SOM with "HUB" configuration; USB3 - USB 2.0 HOST via HUB;		TUSB8041IRGCR.18
S70		GND	GND	Digital Ground;		GND
S71	no HUB	USB2_SSTX+	USB2_TX_P	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal;		SOC.A13
S71	HUB	USB2_SSTX+	USBH_P2_C_SSTXP	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.11

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S72	no HUB	USB2_SSTX-	USB2_TX_N	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal;		SOC.B13
S72	HUB	USB2_SSTX-	USBH_P2_C_SSTXN	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.12
S73		GND	GND	Digital Ground;		GND
S74	no HUB	USB2_SSRX+	USB2_RX_P	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal;		SOC.A12
S74	HUB	USB2_SSRX+	USBH_P2_SSRXP	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.14
S75	no HUB	USB2_SSRX-	USB2_RX_N	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal;		SOC.B12
S75	HUB	USB2_SSRX-	USBH_P2_SSRXN	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB;		TUSB8041IRGCR.15
S76		PCIE_B_RST#	NC			NC
S77	no WRST	PCIE_C_RST#	NC	In "no WRST" configuration this pin is Not Connected;		NC
S77	WRST	PCIE_C_RST#	WB_KILL_1V8	Available in SOM with "WRST" configuration;	1.8V	LBES5PL2xL.63
S78		PCIE_C_RX+ / SERDES_1_RX+	NC			NC
S79		PCIE_C_RX- / SERDES_1_RX-	NC			NC
S80		GND	GND	Digital Ground;		GND
S81	no COEX & no BTRST	PCIE_C_TX+ / SERDES_1_TX+	MIPI_CSI1_D3_P	Available in SOM without "COEX" and without "BTRST" configuration;		SOC.D26
S81	BTRST	PCIE_C_TX+ / SERDES_1_TX+	LR_KILL_1V8	Available in SOM with "BTRST" configuration;	1.8V	LBES5PL2xL.38
S81	COEX & no BTRST	PCIE_C_TX+ / SERDES_1_TX+	NC	In "COEX and no BTRST" configuration this pin is Not Connected;		
S82	no COEX & no BTRST	PCIE_C_TX- / SERDES_1_TX-	MIPI_CSI1_D3_N	Available in SOM without "COEX" and without "BTRST" configuration;		SOC.E26
S82	BTRST	PCIE_C_TX- / SERDES_1_TX-	BT_KILL_1V8	Available in SOM with "BTRST" configuration;	1.8V	LBES5PL2xL.64
S82	COEX & no BTRST	PCIE_C_TX- / SERDES_1_TX-	NC	In "COEX and no BTRST" configuration this pin is Not Connected;		NC
S83		GND	GND	Digital Ground;		GND
S84		PCIE_B_REFCK+	NC			NC
S85		PCIE_B_REFCK-	NC			NC
S86		GND	GND	Digital Ground;		GND

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S87		PCIE_B_RX+	NC			NC
S88		PCIE_B_RX-	NC			NC
S89		GND	GND	Digital Ground;		GND
S90		PCIE_B_TX+	NC			NC
S91		PCIE_B_TX-	NC			NC
S92		GND	GND	Digital Ground;		GND
S93	no DSI2LV	DP0_LANE0+	MIPI_DSI1_D0_P	Available in SOM without "DSI2LV" configuration;		SOC.A16
S93	DSI2LV	DP0_LANE0+	NC			NC
S94	no DSI2LV	DP0_LANE0-	MIPI_DSI1_D0_N	Available in SOM without "DSI2LV" configuration;		SOC.B16
S94	DSI2LV	DP0_LANE0-	NC			NC
S95		DP0_AUX_SEL	NC			NC
S96	no DSI2LV	DP0_LANE1+	MIPI_DSI1_D1_P	Available in SOM without "DSI2LV" configuration;		SOC.A17
S96	DSI2LV	DP0_LANE1+	NC			NC
S97	no DSI2LV	DP0_LANE1-	MIPI_DSI1_D1_N	Available in SOM without "DSI2LV" configuration;		SOC.B17
S97	DSI2LV	DP0_LANE1-	NC			NC
S98		DP0_HPD	NC			NC
S99	no DSI2LV	DP0_LANE2+	MIPI_DSI1_D2_P	Available in SOM without "DSI2LV" configuration;		SOC.A19
S99	DSI2LV	DP0_LANE2+	NC			NC
S100	no DSI2LV	DP0_LANE2-	MIPI_DSI1_D2_N	Available in SOM without "DSI2LV" configuration;		SOC.B19
S100	DSI2LV	DP0_LANE2-	NC			NC
S101		GND	GND	Digital Ground;		GND
S102	no DSI2LV	DP0_LANE3+	MIPI_DSI1_D3_P	Available in SOM without "DSI2LV" configuration;		SOC.A20
S102	DSI2LV	DP0_LANE3+	NC			NC
S103	no DSI2LV	DP0_LANE3-	MIPI_DSI1_D3_N	Available in SOM without "DSI2LV" configuration;		SOC.B20
S103	DSI2LV	DP0_LANE3-	NC			NC
S104		USB3_OTG_ID	NC			NC
S105	no DSI2LV	DP0_AUX+	MIPI_DSI1_CLK_P	Available in SOM without "DSI2LV" configuration;		SOC.A18
S105	DSI2LV	DP0_AUX+	NC			NC

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S106	no DSI2LV	DP0_AUX-	MIPI_DSI1_CLK_N	Available in SOM without "DSI2LV" configuration;		SOC.B18
S106	DSI2LV	DP0_AUX-	NC			NC
S107	no WAKE	LCD1_BKLT_EN	NC	In "no WAKE" configuration this pin is Not Connected;		NC
S107	WAKE	LCD1_BKLT_EN	WIFI_HOST_WAKE_1V8	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2xL.73
S108		LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P			SOC.A28
S109		LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N			SOC.B28
S110		GND	GND	Digital Ground;		GND
S111		LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P			SOC.A26
S112		LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N			SOC.B26
S113	no WAKE	eDP1_HPD / DSI1_TE	NC	In "no WAKE" configuration this pin is Not Connected;		NC
S113	WAKE	eDP1_HPD / DSI1_TE	BT_DEV_WAKE_1V8	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2xL.75
S114		LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P			SOC.A27
S115		LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N			SOC.B27
S116	no WAKE	LCD1_VDD_EN	NC	In "no WAKE" configuration this pin is Not Connected;		NC
S116	WAKE	LCD1_VDD_EN	BT_HOST_WAKE_1V8	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2xL.76
S117		LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P			SOC.B29
S118		LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N			SOC.C28
S119		GND	GND	Digital Ground;		GND
S120		LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P			SOC.C29
S121		LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N			SOC.D28
S122		LCD1_BKLT_PWM	GPIO1_IO11(PWM2_OUT)		1.8V	SOC.D8
S123		GPIO13	SAI2_RXFS(GPIO4_IO21)	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S124		GND	GND	Digital Ground;		GND
S125	no DSI2LV	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_D0_P	Available in SOM without "DSI2LV" configuration;		SOC.D29
S125	DSI2LV	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSI1_D0_P	Available in SOM with "DSI2LV" configuration;		SOC.A16
S126	no DSI2LV	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_D0_N	Available in SOM without "DSI2LV" configuration;		SOC.E28
S126	DSI2LV	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSI1_D0_N	Available in SOM with "DSI2LV" configuration;		SOC.B16
S127		LCD0_BKLT_EN	GPIO_EXP_P0_5__LCD0_BKLT_EN	Signal source is GPIO Expander P0_5;	1.8V	PCAL6416AHF,128.6
S128	no DSI2LV	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_D1_P	Available in SOM without "DSI2LV" configuration;		SOC.E29
S128	DSI2LV	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	MIPI_DSI1_D1_P	Available in SOM with "DSI2LV" configuration;		SOC.A17
S129	no DSI2LV	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_D1_N	Available in SOM without "DSI2LV" configuration;		SOC.F28
S129	DSI2LV	LVDS0_1- / eDP0_TX1- / DSI0_D1-	MIPI_DSI1_D1_N	Available in SOM with "DSI2LV" configuration;		SOC.B17
S130		GND	GND	Digital Ground;		GND
S131	no DSI2LV	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_D2_P	Available in SOM without "DSI2LV" configuration;		SOC.G29
S131	DSI2LV	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSI1_D2_P	Available in SOM with "DSI2LV" configuration;		SOC.A19
S132	no DSI2LV	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_D2_N	Available in SOM without "DSI2LV" configuration;		SOC.H28
S132	DSI2LV	LVDS0_2- / eDP0_TX2- / DSI0_D2-	MIPI_DSI1_D2_N	Available in SOM with "DSI2LV" configuration;		SOC.B19
S133		LCD0_VDD_EN	GPIO_EXP_P0_4__LCD0_VDD_EN	Signal source is GPIO Expander P0_4;	1.8V	PCAL6416AHF,128.5
S134	no DSI2LV	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CLK_P	Available in SOM without "DSI2LV" configuration;		SOC.F29
S134	DSI2LV	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	MIPI_DSI1_CLK_P	Available in SOM with "DSI2LV" configuration;		SOC.A18
S135	no DSI2LV	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CLK_N	Available in SOM without "DSI2LV" configuration;		SOC.G28
S135	DSI2LV	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	MIPI_DSI1_CLK_N	Available in SOM with "DSI2LV" configuration;		SOC.B18
S136		GND	GND	Digital Ground;		GND

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S137	no DSI2LV	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_D3_P	Available in SOM without "DSI2LV" configuration;		SOC.H29
S137	DSI2LV	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	MIPI_DSI1_D3_P	Available in SOM with "DSI2LV" configuration;		SOC.A20
S138	no DSI2LV	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_D3_N	Available in SOM without "DSI2LV" configuration;		SOC.J28
S138	DSI2LV	LVDS0_3- / eDP0_TX3- / DSI0_D3-	MIPI_DSI1_D3_N	Available in SOM with "DSI2LV" configuration;		SOC.B20
S139		I2C_LCD_CK	SAI5_RXFS(I2C6_SCL)	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
S140		I2C_LCD_DAT	SAI5_RXC(I2C6_SDA)	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(PWM1_OUT)		1.8V	SOC.AC18
S142		GPIO12	SAI2_RXC(GPIO4_IO22)	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S143		GND	GND	Digital Ground;		GND
S144		eDP0_HPD / DSI0_TE	NC			NC
S145		WDT_TIME_OUT#	WDOG_B		1.8V	SOC.B6
S146		PCIE_WAKE#	GPIO_EXP_P1_7__PCIE_WAKE#_3V3	Signal source is GPIO Expander P1_7;	3.3V, via bidirectional OD level shifter; with 10K PU	PCAL6416AHF,128.17 (via bidirectional OD level shifter)
S147		VDD_RTC	VBAT_RTC	RTC Power input;	1.2V-5.5V	VDD_RTC
S148		LID#	SAI1_TXD6(GPIO4_IO18)		1.8V; PU 10K	SOC.AC12
S149		SLEEP#	SAI1_RXFS(GPIO4_IO00)		1.8V; PU 10K	SOC.AJ9
S150		VIN_PWR_BAD#	PMIC_ON_REQ (via diode)		1.8V to VDD_IN, Input via diode; PU 100K	PCA9450CHNY.39 via diode;
S151	no CHG	CHARGING#	NC	In "no CHG" configuration this pin is Not Connected;		NC
S151	CHG	CHARGING#	SAI2_RXFS(GPIO4_IO21)	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
S152	no CHG	CHARGER_PRSNT#	NC	In "no CHG" configuration this pin is Not Connected;		NC
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(GPIO4_IO22)	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
S153		CARRIER_STBY#	PMIC_STBY_REQ_B	PMIC_STBY_REQ (Via inverting FET);	1.8V	SOC.J24 (Via inv. FET)

Pin	Assembly	SMARC pin name	SOM Pin name (function)	Notes	I/O Level; PU/PD	Ball
S154		CARRIER_PWR_ON	CARRIER_PWR_ON	SOM Peripherals' 3.3v rail Output Via resistor divider;	1.8V	SOM_3V3_PER (Via res. divider)
S155		FORCE_RECOV#	FORCE_RECOV#	Boot device to be rewritten / restored from an external USB Host on Module USB0, implemented with internal logic;	1.8V; PU 10K	
S156	no CHG	BATLOW#	NC	In "no CHG" configuration this pin is Not Connected;		NC
S156	CHG	BATLOW#	GPIO1_IO06	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
S157		TEST#	JTAG_MOD		1.8V	SOC.G20
S158		GND	GND	Digital Ground;		GND

7.5 VAR-SMARC-MX8M-PLUS Connector Pin Mux

Table 3: VAR-SMARC-MX8M-PLUS Connector PINMUX

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
P1		SOC.AJ13	SAI1_TX_DATA7	SAI6_MCLK		PDM_CLK	ENET1_TX_ER	GPIO4_IO19	
P5		SOC.AH8 (via push pull level shifter)	SAI1_RX_BCLK			PDM_CLK	ENET1_1588_EVENT0_OUT	GPIO4_IO01	
P6		SOC.B8 (via push pull level shifter)	GPIO1_IO09	ENET_QOS_1588_EVENT0_ OUT	PWM2_OUT	ISP_SHUTTER_OPEN_1	USDHC3_RESET_B	SDMA2_EXT_EVENT0	
P19	no EC1	SOC.AF28	ENET_QOS_RGMII_RD3		SAI7_MCLK	SPDIF1_IN		GPIO1_IO29	USDHC3_CMD
P20	no EC1	SOC.AF29	ENET_QOS_RGMII_RD2		SAI7_RX_BCLK	PDM_CLK		GPIO1_IO28	USDHC3_CLK
P21	no EC1	SOC.AE24	ENET_QOS_RGMII_TXC	ENET_QOS_TX_ER	SAI7_TX_DATA0			GPIO1_IO23	USDHC3_DATA1
P22	no EC1	SOC.AE29	ENET_QOS_RGMII_RXC	ENET_QOS_RX_ER	SAI7_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO25	USDHC3_DATA3
P23	no EC1	SOC.AG28	ENET_QOS_RGMII_RD1		SAI7_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO27	USDHC3_RESET_B
P24	no EC1	SOC.AG29	ENET_QOS_RGMII_RD0		SAI7_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO26	USDHC3_DATA4
P25	no EC1	SOC.AE28	ENET_QOS_RGMII_RX_CTL		SAI7_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO24	USDHC3_DATA2
P26	no EC1	SOC.AC25	ENET_QOS_RGMII_TD0		SAI6_RX_BCLK	PDM_CLK		GPIO1_IO21	USDHC3_WP
P27	no EC1	SOC.AE26	ENET_QOS_RGMII_TD1		SAI6_RX_SYNC	PDM_BIT_STREAM0		GPIO1_IO20	USDHC3_CD_B
P29	no EC1	SOC.AF26	ENET_QOS_RGMII_TD2	ENET_QOS_INPUT=ENET_ QOS_TX_CLK OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT	SAI6_RX_DATA0	PDM_BIT_STREAM1		GPIO1_IO19	USDHC3_DATA7
P30	no EC1	SOC.AD24	ENET_QOS_RGMII_TD3		SAI6_TX_BCLK	PDM_BIT_STREAM2		GPIO1_IO18	USDHC3_DATA6
P31		SOC.AE12	SAI1_MCLK		SAI1_TX_BCLK		ENET1_INPUT=ENET1_TX_ CLK OUTPUT=CCM_ENET_REF_ CLK_ROOT	GPIO4_IO20	
P33		SOC.AC26	USDHC2_WP					GPIO2_IO20	
P34		SOC.AB28	USDHC2_CMD		ECSPI2_MOSI	UART4_TX	PDM_CLK	GPIO2_IO14	
P35		SOC.AD29	USDHC2_CD_B					GPIO2_IO12	
P36		SOC.AB29	USDHC2_CLK		ECSPI2_SCLK	UART4_RX		GPIO2_IO13	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
P37		SOC.A8 (via push pull level shifter)	GPIO1_IO08	ENET_QOS_1588_EVENT0_ IN	PWM1_OUT	ISP_PRELIGHT_TRIG_1	ENET_QOS_1588_EVENT0_ AUX_IN	USDHC2_RESET_B	
P39		SOC.AC28	USDHC2_DATA0		I2C4_SDA	UART2_RX	PDM_BIT_STREAM0	GPIO2_IO15	
P40		SOC.AC29	USDHC2_DATA1		I2C4_SCL	UART2_TX	PDM_BIT_STREAM1	GPIO2_IO16	
P41		SOC.AA26	USDHC2_DATA2		ECSPI2_SS0	SPDIF1_OUT	PDM_BIT_STREAM2	GPIO2_IO17	
P42		SOC.AA25	USDHC2_DATA3		ECSPI2_MISO	SPDIF1_IN	PDM_BIT_STREAM3	GPIO2_IO18	SRC_EARLY_RESET
P43	no WBE	SOC.AE8	I2C2_SDA	ENET_QOS_1588_EVENT1_ OUT	USDHC3_WP	ECSPI1_SS0		GPIO5_IO17	
P43	WBE	SOC.A7	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		CCM_REF_CLK_32K	CCM_EXT_CLK1
P44		SOC.AC8	I2C1_SCL	ENET_QOS_MDC		ECSPI1_SCLK		GPIO5_IO14	
P45		SOC.AH6	I2C2_SCL	ENET_QOS_1588_EVENT1_ IN	USDHC3_CD_B	ECSPI1_MISO	ENET_QOS_1588_EVENT1_ AUX_IN	GPIO5_IO16	
P46		SOC.AH7	I2C1_SDA	ENET_QOS_MDIO		ECSPI1_MOSI		GPIO5_IO15	
P54	no QSPI	SOC.AJ22	ECSPI2_SS0	UART4_RTS_B	I2C4_SDA		CCM_CLKO2	GPIO5_IO13	
P54	QSPI	SOC.L26	NAND_CE0_B	QSPI_A_SS0_B	SAI3_TX_DATA0	ISP_SHUTTER_TRIG_0	UART3_TX	GPIO3_IO01	
P55		SOC.R26	NAND_DQS	QSPI_A_DQS	SAI3_MCLK	ISP_SHUTTER_OPEN_0	I2C3_SCL	GPIO3_IO14	
P56	no QSPI	SOC.AH21	ECSPI2_SCLK	UART4_RX	I2C3_SCL	SAI7_TX_BCLK		GPIO5_IO10	
P56	QSPI	SOC.N25	NAND_ALE	QSPI_A_SCLK	SAI3_TX_BCLK	ISP_FL_TRIG_0	UART3_RX	GPIO3_IO00	
P57	no QSPI	SOC.AH20	ECSPI2_MISO	UART4_CTS_B	I2C4_SCL	SAI7_MCLK	CCM_CLKO1	GPIO5_IO12	
P57	QSPI	SOC.L25	NAND_DATA01	QSPI_A_DATA1	SAI3_TX_SYNC	ISP_PRELIGHT_TRIG_0	UART4_TX	GPIO3_IO07	
P58	no QSPI	SOC.AJ21	ECSPI2_MOSI	UART4_TX	I2C3_SDA	SAI7_TX_DATA0		GPIO5_IO11	
P58	QSPI	SOC.R25	NAND_DATA00	QSPI_A_DATA0	SAI3_RX_DATA0	ISP_FLASH_TRIG_0	UART4_RX	GPIO3_IO06	
P62		SOC.A6 (via bidirectional OD level shifter)	GPIO1_IO13	USB1_OTG_OC				PWM2_OUT	
P64		SOC.B7 (via push pull level shifter)	GPIO1_IO10	USB1_OTG_ID	PWM3_OUT				
P104		SOC.AE22	HDMI_HPD	HDMI_HPD_O		I2C6_SDA	FLEXCAN2_RX	GPIO3_IO29	
P105		SOC.AC22	HDMI_SCL			I2C5_SCL	FLEXCAN1_TX	GPIO3_IO26	
P106		SOC.AF22	HDMI_SDA			I2C5_SDA	FLEXCAN1_RX	GPIO3_IO27	
P112		SOC.D6	GPIO1_IO03	USDHC1_VSELECT		ISP_PRELIGHT_TRIG_0		SDMA1_EXT_EVENT0	
P113		SOC.A4	GPIO1_IO14	USB2_OTG_PWR			USDHC3_CD_B	PWM3_OUT	CCM_CLKO1
P114		SOC.B4	GPIO1_IO05	M7_NMI		ISP_FL_TRIG_1		CCM_PMIC_READY	

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
P115		SOC.A7	GPIO1_IO00	CCM_ENET_PHY_REF_CLK_ROOT		ISP_FL_TRIG_0		CCM_REF_CLK_32K	CCM_EXT_CLK1
P116		SOC.AC10	SAI1_RX_DATA0		SAI1_TX_DATA1	PDM_BIT_STREAM0	ENET1_1588_EVENT1_IN	GPIO4_IO02	
P117		SOC.E8	GPIO1_IO01	PWM1_OUT		ISP_SHUTTER_TRIG_0		CCM_REF_CLK_24M	CCM_EXT_CLK2
P118		SOC.F6	GPIO1_IO07	ENET_QOS_MDIO		ISP_FLASH_TRIG_1		USDHC1_WP	CCM_EXT_CLK4
P119		SOC.A3	GPIO1_IO06	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		USDHC1_CD_B	CCM_EXT_CLK3
P121		SOC.AA28	USDHC1_DATA6	ENET1_RGMII_RX_CTL		I2C2_SCL	UART3_TX	GPIO2_IO08	
P122		SOC.U25	USDHC1_DATA7	ENET1_RX_ER		I2C2_SDA	UART3_RX	GPIO2_IO09	
P129		SOC.AJ3	UART1_TX	ECSPI3_MOSI				GPIO5_IO23	
P130		SOC.AD6	UART1_RX	ECSPI3_SCLK				GPIO5_IO22	
P131		SOC.AE6	UART3_RX	UART1_CTS_B	USDHC3_RESET_B	GPT1_CAPTURE2	FLEXCAN2_TX	GPIO5_IO26	
P132		SOC.AJ4	UART3_TX	UART1_RTS_B	USDHC3_VSELECT	GPT1_CLK	FLEXCAN2_RX	GPIO5_IO27	
P134		SOC.AH4	UART2_TX	ECSPI3_SS0		GPT1_COMPARE2		GPIO5_IO25	
P135		SOC.AF6	UART2_RX	ECSPI3_MISO		GPT1_COMPARE3		GPIO5_IO24	
P136		SOC.AC20	ECSPI1_MOSI	UART3_TX	I2C1_SDA	SAI7_RX_BCLK		GPIO5_IO07	
P137		SOC.AF20	ECSPI1_SCLK	UART3_RX	I2C1_SCL	SAI7_RX_SYNC		GPIO5_IO06	
P138		SOC.AD20	ECSPI1_MISO	UART3_CTS_B	I2C2_SCL	SAI7_RX_DATA0		GPIO5_IO08	
P139		SOC.AE20	ECSPI1_SS0	UART3_RTS_B	I2C2_SDA	SAI7_TX_SYNC		GPIO5_IO09	
P140		SOC.AH5	UART4_TX	UART2_RTS_B		GPT1_CAPTURE1	I2C6_SDA	GPIO5_IO29	
P141		SOC.AJ5	UART4_RX	UART2_CTS_B	PCIE1_CLKREQ_B	GPT1_COMPARE1	I2C6_SCL	GPIO5_IO28	
P143		SOC.AE18	SPDIF1_OUT	PWM3_OUT	I2C5_SCL	GPT1_COMPARE1	FLEXCAN1_TX	GPIO5_IO03	
P144		SOC.AD18	SPDIF1_IN	PWM2_OUT	I2C5_SDA	GPT1_COMPARE2	FLEXCAN1_RX	GPIO5_IO04	
P145		SOC.AD22	HDMI_CEC			I2C6_SCL	FLEXCAN2_TX	GPIO3_IO28	
P146		SOC.AF14	SAI5_MCLK	SAI1_TX_BCLK	PWM1_OUT	I2C5_SDA		GPIO3_IO25	FLEXCAN2_RX
S1		SOC.AC14	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL		GPIO3_IO19	
S2		SOC.AD14	SAI5_RX_BCLK	SAI1_TX_DATA1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20	
S5		SOC.AJ7	I2C3_SCL	PWM4_OUT	GPT2_CLK	ECSPI2_SCLK		GPIO5_IO18	
S6		SOC.B5	GPIO1_IO15	USB2_OTG_OC			USDHC3_WP	PWM4_OUT	CCM_CLKO2
S7		SOC.AJ6	I2C3_SDA	PWM3_OUT	GPT3_CLK	ECSPI2_MOSI		GPIO5_IO19	
S38		SOC.AJ15	SAI2_MCLK	SAI5_MCLK	ENET_QOS_1588_EVENT3_IN	FLEXCAN2_RX	ENET_QOS_1588_EVENT3_AUX_IN	GPIO4_IO27	SAI3_MCLK
S39		SOC.AJ17	SAI2_TX_SYNC	SAI5_TX_DATA1	ENET_QOS_1588_EVENT3_OUT	SAI2_TX_DATA1	UART1_CTS_B	GPIO4_IO24	PDM_BIT_STREAM2
S40		SOC.AH16	SAI2_TX_DATA0	SAI5_TX_DATA3	ENET_QOS_1588_EVENT2_IN	FLEXCAN2_TX	ENET_QOS_1588_EVENT2_AUX_IN	GPIO4_IO26	SRC_BOOT_MODE4

Pin	Assembly	Ball	ALT0	ALT1	ALT2	ALT3	ALT4	ALT5	ALT6
S41		SOC.AJ14	SAI2_RX_DATA0	SAI5_TX_DATA0	ENET_QOS_1588_EVENT2_OUT	SAI2_TX_DATA1	UART1_RTS_B	GPIO4_IO23	PDM_BIT_STREAM3
S42		SOC.AH15	SAI2_TX_BCLK	SAI5_TX_DATA2		FLEXCAN1_RX		GPIO4_IO25	PDM_BIT_STREAM1
S43	no AC & SAI3	SOC.AJ19	SAI3_RX_SYNC	SAI2_RX_DATA1	SAI5_RX_SYNC	SAI3_RX_DATA1	SPDIF1_IN	GPIO4_IO28	PDM_BIT_STREAM0
S44	no AC & SAI3	SOC.AJ18	SAI3_RX_BCLK	SAI2_RX_DATA2	SAI5_RX_BCLK	GPT1_CLK	UART2_CTS_B	GPIO4_IO29	PDM_CLK
S45		SOC.AH28	ENET_QOS_MDC		SAI6_TX_DATA0			GPIO1_IO16	USDHC3_STROBE
S46		SOC.AH29	ENET_QOS_MDIO		SAI6_TX_SYNC	PDM_BIT_STREAM3		GPIO1_IO17	USDHC3_DATA5
S48		SOC.AF8	I2C4_SCL	PWM2_OUT	PCIE1_CLKREQ_B	ECSPI2_MISO		GPIO5_IO20	
S49		SOC.AD8	I2C4_SDA	PWM1_OUT		ECSPI2_SS0		GPIO5_IO21	
S50	no AC	SOC.AC16	SAI3_TX_SYNC	SAI2_TX_DATA1	SAI5_RX_DATA1	SAI3_TX_DATA1	UART2_RX	GPIO4_IO31	PDM_BIT_STREAM3
S51	no AC	SOC.AH18	SAI3_TX_DATA0	SAI2_TX_DATA3	SAI5_RX_DATA3	GPT1_CAPTURE2	SPDIF1_EXT_CLK	GPIO5_IO01	SRC_BOOT_MODE5
S52	no AC	SOC.AF18	SAI3_RX_DATA0	SAI2_RX_DATA3	SAI5_RX_DATA0		UART2_RTS_B	GPIO4_IO30	PDM_BIT_STREAM1
S53	no AC	SOC.AH19	SAI3_TX_BCLK	SAI2_TX_DATA2	SAI5_RX_DATA2	GPT1_CAPTURE1	UART2_TX	GPIO5_IO00	PDM_BIT_STREAM2
S54	no EC1	SOC.AH13	ENET_QOS_RGMII_TX_CTL		SAI6_MCLK	SPDIF1_OUT		GPIO1_IO22	USDHC3_DATA0
S56	QSPI	SOC.L24	NAND_DATA02	QSPI_A_DATA2	USDHC3_CD_B	UART4_CTS_B	I2C4_SDA	GPIO3_IO08	
S57	QSPI	SOC.N24	NAND_DATA03	QSPI_A_DATA3	USDHC3_WP	UART4_RTS_B	ISP_FL_TRIG_1	GPIO3_IO09	
S58	no AC & SAI3	SOC.AJ20	SAI3_MCLK	PWM4_OUT	SAI5_MCLK		SPDIF1_OUT	GPIO5_IO02	SPDIF1_IN
S122		SOC.D8	GPIO1_IO11	USB2_OTG_ID	PWM2_OUT		USDHC3_VSELECT	CCM_PMIC_READY	
S123		SOC.AH17	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM3
S139		SOC.AC14	SAI5_RX_SYNC	SAI1_TX_DATA0	PWM4_OUT	I2C6_SCL		GPIO3_IO19	
S140		SOC.AD14	SAI5_RX_BCLK	SAI1_TX_DATA1	PWM3_OUT	I2C6_SDA	PDM_CLK	GPIO3_IO20	
S141		SOC.AC18	SPDIF1_EXT_CLK	PWM1_OUT		GPT1_COMPARE3		GPIO5_IO05	
S142		SOC.AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1
S145		SOC.B6	GPIO1_IO02	WDOG1_WDOG_B		ISP_FLASH_TRIG_0		WDOG1_WDOG_ANY	
S148		SOC.AC12	SAI1_TX_DATA6	SAI6_RX_SYNC	SAI6_TX_SYNC		ENET1_RX_ER	GPIO4_IO18	
S149		SOC.AJ9	SAI1_RX_SYNC				ENET1_1588_EVENT0_IN	GPIO4_IO00	
S151	CHG	SOC.AH17	SAI2_RX_SYNC	SAI5_TX_SYNC	SAI5_TX_DATA1	SAI2_RX_DATA1	UART1_TX	GPIO4_IO21	PDM_BIT_STREAM3
S152	CHG	SOC.AJ16	SAI2_RX_BCLK	SAI5_TX_BCLK		FLEXCAN1_TX	UART1_RX	GPIO4_IO22	PDM_BIT_STREAM1
S156	CHG	SOC.A3	GPIO1_IO06	ENET_QOS_MDC		ISP_SHUTTER_TRIG_1		USDHC1_CD_B	CCM_EXT_CLK3

8. SOM's Interfaces

8.1 Trace Impedance

SOM traces are designed with the below table impedance list per signal group.
Table is a reference when you are updating or creating constraints in the PCB design tool to set up the impedances/trace widths.

Table 4: SOM Signal Group Traces Impedance

Signal Group	Impedance
All single ended signals	50 Ω Single ended
PCIe Clock, TX/RX data pairs	85 Ω Differential
USB Differential signals	90 Ω Differential
Differential signals including: Ethernet, MIPI (CSI and DSI), LVDS, HDMI	100 Ω Differential

8.2 Display Interfaces

the i.MX 8M Plus SoC has the following display support

- Three LCDIF Display Controllers:
    o One LCDIF drives MIPI DSI
    o One LCDIF drives LVDS Tx
    o One LCDIF drives HDMI Tx

Support up to 1920x1200p60 display per LCDIF if no more than 2 instances are used simultaneously, or 2x 1080p60 + 1x 4kp30 on HDMI if all 3 instances are used simultaneously.

The VAR-SMARC-MX8M-PLUS supports all display interfaces HDMI, MIPI DSI and LVDS display available by the i.MX 8M Plus SoC

8.2.1 HDMI

The following features are supported:

HDMI 2.0a Tx supporting one display

- Resolutions of: 720 x 480p60, 1280 x 720p60, 1920 x 1080p60, 1920 x 1080p120,
- 3840 x 2160p30
- Pixel clock up to 297 MHz

Audio support

- 32 channel audio output support
- 1 S/PDIF audio eARC input support

The SMARC specification defines 1x HDMI display interfaces with its control signal which is mapped to the i.MX 8M Plus SoC HDMI interface.

8.2.1.1 HDMI Signals -SMARC HDMI pinout

Table 5: HDMI Signals - SMARC HDMI pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P92		HDMI_D2+ / DP1_LANE0+	HDMI_TX2_P	0	Differential Pair Positive side;		SOC.AH27
P93		HDMI_D2- / DP1_LANE0-	HDMI_TX2_N	0	Differential Pair Negative side;		SOC.AJ27
P95		HDMI_D1+ / DP1_LANE1+	HDMI_TX1_P	0	Differential Pair Positive side;		SOC.AH26
P96		HDMI_D1- / DP1_LANE1-	HDMI_TX1_N	0	Differential Pair Negative side;		SOC.AJ26
P98		HDMI_D0+ / DP1_LANE2+	HDMI_TX0_P	0	Differential Pair Positive side;		SOC.AH25
P99		HDMI_D0- / DP1_LANE2-	HDMI_TX0_N	0	Differential Pair Negative side;		SOC.AJ25
P101		HDMI_CK+ / DP1_LANE3+	HDMI_TXC_P	0	Differential Pair Positive side;		SOC.AH24
P102		HDMI_CK- / DP1_LANE3-	HDMI_TXC_N	0	Differential Pair Negative side;		SOC.AJ24
P104		HDMI_HPD / DP1_HPD	HDMI_HPD	0		1.8V	SOC.AE22
P105		HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL(HDMI_SCL)	0		1.8V	SOC.AC22
P106		HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA(HDMI_SDA)	0		1.8V	SOC.AF22

8.2.2 LVDS

The LVDS Display Bridge (LDB) connects the CPU internal LCDIF to External LVDS Display. The purpose of the LDB is to support flow of synchronous RGB data to external display devices through the LVDS interface.

The LVDS ports can be used as follows:

- Single channel (4 lanes) supports resolutions up to 720p60
- Dual asynchronous channels (8 data, 2 clocks). Supports resolutions up to 1920x1200p60 This is intended for a single panel with two interfaces, transferring across two channels (even pixel/odd pixel).

The Pixel Mapper splits and reorders the pixels from the single LCDIF display output into an odd and even pixel stream. Splitting and reordering is required to match the LVDS Displays speed and channel requirements. Both VESA and JEIDA pixel mapping is supported.

The SMARC specification defines 2x LVDS LVDS0/1display interfaces with their control signal, both are mapped to the i.MX 8M Plus SoC LVDS0/1 interfaces and PWM, GPIOs.

8.2.2.1 LVDS0 Signals – SMARC LVDS0 pinout

Table 6: LVDS0 Signals – SMARC LVDS0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S125	no DSI2LV	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	LVDS0_D0_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.D29
S126	no DSI2LV	LVDS0_0- / eDP0_TX0- / DSI0_D0-	LVDS0_D0_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.E28
S128	no DSI2LV	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	LVDS0_D1_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.E29
S129	no DSI2LV	LVDS0_1- / eDP0_TX1- / DSI0_D1-	LVDS0_D1_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.F28
S131	no DSI2LV	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	LVDS0_D2_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.G29
S132	no DSI2LV	LVDS0_2- / eDP0_TX2- / DSI0_D2-	LVDS0_D2_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.H28
S134	no DSI2LV	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	LVDS0_CLK_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.F29
S135	no DSI2LV	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	LVDS0_CLK_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.G28
S137	no DSI2LV	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	LVDS0_D3_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.H29
S138	no DSI2LV	LVDS0_3- / eDP0_TX3- / DSI0_D3-	LVDS0_D3_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.J28

8.2.2.2   LVDS1 Signals – SMARC LVDS1 pinout

Table 7: LVDS1 Signals – SMARC LVDS1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S108		LVDS1_CK+ / eDP1_AUX+ / DSI1_CLK+	LVDS1_CLK_P	0	Differential Pair Positive side;		SOC.A28
S109		LVDS1_CK- / eDP1_AUX- / DSI1_CLK-	LVDS1_CLK_N	0	Differential Pair Negative side;		SOC.B28
S111		LVDS1_0+ / eDP1_TX0+ / DSI1_D0+	LVDS1_D0_P	0	Differential Pair Positive side;		SOC.A26
S112		LVDS1_0- / eDP1_TX0- / DSI1_D0-	LVDS1_D0_N	0	Differential Pair Negative side;		SOC.B26
S114		LVDS1_1+ / eDP1_TX1+ / DSI1_D1+	LVDS1_D1_P	0	Differential Pair Positive side;		SOC.A27
S115		LVDS1_1- / eDP1_TX1- / DSI1_D1-	LVDS1_D1_N	0	Differential Pair Negative side;		SOC.B27
S117		LVDS1_2+ / eDP1_TX2+ / DSI1_D2+	LVDS1_D2_P	0	Differential Pair Positive side;		SOC.B29
S118		LVDS1_2- / eDP1_TX2- / DSI1_D2-	LVDS1_D2_N	0	Differential Pair Negative side;		SOC.C28
S120		LVDS1_3+ / eDP1_TX3+ / DSI1_D3+	LVDS1_D3_P	0	Differential Pair Positive side;		SOC.C29
S121		LVDS1_3- / eDP1_TX3- / DSI1_D3-	LVDS1_D3_N	0	Differential Pair Negative side;		SOC.D28

8.2.2.3   LVDS0/1 control Signals – SMARC LCD0/1 pinout

Table 8: LVDS0/1 control Signals – SMARC LCD0/1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S139		I2C_LCD_CK	SAI5_RXFS(I2C6_SCL)	3	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
S140		I2C_LCD_DAT	SAI5_RXC(I2C6_SDA)	3	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
S127		LCD0_BKLT_EN	GPIO_EXP_P0_5__LCD0_BKLT_EN	0	Signal source is GPIO Expander P0_5;	1.8V	PCAL6416AHF,128.6
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(PWM1_OUT)	1		1.8V	SOC.AC18
S133		LCD0_VDD_EN	GPIO_EXP_P0_4__LCD0_VDD_EN	0	Signal source is GPIO Expander P0_4;	1.8V	PCAL6416AHF,128.5
S107	WAKE	LCD1_BKLT_EN	WIFI_HOST_WAKE_1V8	0	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2xL.73
S122		LCD1_BKLT_PWM	GPIO1_IO11(PWM2_OUT)	2		1.8V	SOC.D8
S116	WAKE	LCD1_VDD_EN	BT_HOST_WAKE_1V8	0	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2xL.76

8.2.3 DSI

The i.MX 8M Plus incorporates the MIPI DSI Host Controller.

The key features of the MIPI DSI include:

- Compliant to MIPI-DSI standard v1.2
- Support up to 4 data lanes
- Maximum resolution limited to resolutions achievable with a 250MHz pixel clock and active pixel rate of 200Mpixel/s with 24-bit RGB. This includes resolutions such as:
  - o 1080 p60
  - o WUXGA (1920x1200) at 60 Hz
  - o 1920x1440 at 60 Hz
  - o UWHD (2560x1080) at 60 Hz
  - o WQHD (2560x1440) can be supported by reduced blanking mode
- Support 80Mbps - 1.5Gbps data rate in high speed operation
- Support 10Mbps data rate in low power operation

The SMARC specification defines 2x DSI display interfaces, 1x of which is which is can be achieved through the i.MX 8M Plus SoC DSI interface.

Note: By default, DSI is exported on SMARC DP0 pins; In "DSI2LV" configuration, DSI will not be exported on DP0 pins but instead will be exported from LVDS0 pins

8.2.3.1 DSI Signals – Proprietary SOM pinout (Non-SMARC)

Table 9: MIPI DSI Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S93	no DSI2LV	DP0_LANE0+	MIPI_DSI1_D0_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.A16
S94	no DSI2LV	DP0_LANE0-	MIPI_DSI1_D0_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.B16
S96	no DSI2LV	DP0_LANE1+	MIPI_DSI1_D1_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.A17
S97	no DSI2LV	DP0_LANE1-	MIPI_DSI1_D1_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.B17
S99	no DSI2LV	DP0_LANE2+	MIPI_DSI1_D2_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.A19
S100	no DSI2LV	DP0_LANE2-	MIPI_DSI1_D2_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.B19
S102	no DSI2LV	DP0_LANE3+	MIPI_DSI1_D3_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.A20
S103	no DSI2LV	DP0_LANE3-	MIPI_DSI1_D3_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.B20

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S105	no DSI2LV	DP0_AUX+	MIPI_DSI1_CLK_P	0	Available in SOM without "DSI2LV" configuration; Differential Pair Positive side;		SOC.A18
S106	no DSI2LV	DP0_AUX-	MIPI_DSI1_CLK_N	0	Available in SOM without "DSI2LV" configuration; Differential Pair Negative side;		SOC.B18

8.2.3.2 DSI Signals – SMARC DSI0 pinout

Table 10: MIPI DSI Signals – SMARC DSI0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S125	DSI2LV	LVDS0_0+ / eDP0_TX0+ / DSI0_D0+	MIPI_DSI1_D0_P	0	Available in SOM with "DSI2LV" configuration; Differential Pair Positive side;		SOC.A16
S126	DSI2LV	LVDS0_0- / eDP0_TX0- / DSI0_D0-	MIPI_DSI1_D0_N	0	Available in SOM with "DSI2LV" configuration; Differential Pair Negative side;		SOC.B16
S128	DSI2LV	LVDS0_1+ / eDP0_TX1+ / DSI0_D1+	MIPI_DSI1_D1_P	0	Available in SOM with "DSI2LV" configuration; Differential Pair Positive side;		SOC.A17
S129	DSI2LV	LVDS0_1- / eDP0_TX1- / DSI0_D1-	MIPI_DSI1_D1_N	0	Available in SOM with "DSI2LV" configuration; Differential Pair Negative side;		SOC.B17
S131	DSI2LV	LVDS0_2+ / eDP0_TX2+ / DSI0_D2+	MIPI_DSI1_D2_P	0	Available in SOM with "DSI2LV" configuration; Differential Pair Positive side;		SOC.A19
S132	DSI2LV	LVDS0_2- / eDP0_TX2- / DSI0_D2-	MIPI_DSI1_D2_N	0	Available in SOM with "DSI2LV" configuration; Differential Pair Negative side;		SOC.B19
S134	DSI2LV	LVDS0_CK+ / eDP0_AUX+ / DSI0_CLK+	MIPI_DSI1_CLK_P	0	Available in SOM with "DSI2LV" configuration; Differential Pair Positive side;		SOC.A18
S135	DSI2LV	LVDS0_CK- / eDP0_AUX- / DSI0_CLK-	MIPI_DSI1_CLK_N	0	Available in SOM with "DSI2LV" configuration; Differential Pair Negative side;		SOC.B18
S137	DSI2LV	LVDS0_3+ / eDP0_TX3+ / DSI0_D3+	MIPI_DSI1_D3_P	0	Available in SOM with "DSI2LV" configuration; Differential Pair Positive side;		SOC.A20
S138	DSI2LV	LVDS0_3- / eDP0_TX3- / DSI0_D3-	MIPI_DSI1_D3_N	0	Available in SOM with "DSI2LV" configuration; Differential Pair Negative side;		SOC.B20

8.3   Camera Interface

8.3.1   MIPI CSI-2

The VAR-SMARC-MX8M-PLUS consists of 2x MIPI CSI-2 Host Controller which implements the protocol functions defined in the MIPI CSI-2 specification, allowing communication with an MIPI CSI-2 compliant camera sensor.

The MIPI CSI-2 controller supports the following features:

- MIPI D-PHY specification V1.2 (Board Approved)
- Compliant to MIPI CSI2 Specification V1.3 except for C-PHY feature (Board Approved)
- Support primary and secondary Image format
  - YUV420, YUV420 (Legacy), YUV420 (CSPS), YUV422 of 8-bits and 10-bits
  - RGB565, RGB666, RGB888
  - RAW6, RAW7, RAW8, RAW10, RAW12, RAW14
  - All of User defined Byte-based Data packet
- Support up to 4 lanes of D-PHY operating up to a maximum bit rate of 1.5 Gbps
- Interfaces
  - Compatible to PPI (Protocol-to-PHY Interface) in MIPI D-PHY Specification
  - AMBA3.0 APB Slave for Register configuration.
  - Image output data buswidth: 32 bits
- Image memory size of SRAM is 4KB
- Pixel clock can be gated when no ppi data is coming

The SMARC specification defines up to four MIPI CSI serial camera interfaces.

The SMARC CSI0 interface is mapped to the i.MX8M-PLUS SoC CSI1 interface.
Note - The SMARC CSI0_D[2:3]+/- signals are exported on unused SMARC pins PCIE_C.

The SMARC CSI1 is implemented with four differential data lanes to support higher resolution cameras and is mapped to the i.MX8M-PLUS SoC CSI2 interface.

8.3.1.1   MIPI CSI1 Signals – SMARC CSI0 pinout

Table 11: MIPI CSI1 Signals - SMARC CSI0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S9		CSI0_CK-	MIPI_CSI1_CLK_N	0	Differential Pair Negative side;		SOC.E22
S8		CSI0_CK+	MIPI_CSI1_CLK_P	0	Differential Pair Positive side;		SOC.D22
S12		CSI0_RX0-	MIPI_CSI1_D0_N	0	Differential Pair Negative side;		SOC.E18
S11		CSI0_RX0+	MIPI_CSI1_D0_P	0	Differential Pair Positive side;		SOC.D18
S15		CSI0_RX1-	MIPI_CSI1_D1_N	0	Differential Pair Negative side;		SOC.E20
S14		CSI0_RX1+	MIPI_CSI1_D1_P	0	Differential Pair Positive side;		SOC.D20
P108		GPIO0 / CAM0_PWR#	GPIO_EXP_P0_0__GPIO0_CAM0_PWR#	0	Signal source is GPIO Expander P0_0;	1.8V	PCAL6416 AHF,128.1

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P110		GPIO2 / CAM0_RST#	GPIO_EXP_P0_2__GPIO2_CAM0_RST#	0	Signal source is GPIO Expander P0_2;	1.8V	PCAL6416 AHF,128.3
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(I2C3_SCL)	0		1.8V; PU 2.2K	SOC.AJ7
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(I2C3_SDA)	0		1.8V; PU 2.2K	SOC.AJ6

8.3.1.2 MIPI CSI1 Signals – MIPI CSI1 Proprietary SOM pinout (Non-SMARC)

Table 12: MIPI CSI1 Signals – MIPI CSI1 Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P81	no COEX & no BTRST	PCIE_C_REFCK-	MIPI_CSI1_D2_N	0	Available in SOM without "COEX" and without "BTRST" configuration; Differential Pair Negative side;		SOC.E24
P80	no COEX & no BTRST	PCIE_C_REFCK+	MIPI_CSI1_D2_P	0	Available in SOM without "COEX" and without "BTRST" configuration; Differential Pair Positive side;		SOC.D24
S82	no COEX & no BTRST	PCIE_C_TX- / SERDES_1_TX-	MIPI_CSI1_D3_N	0	Available in SOM without "COEX" and without "BTRST" configuration; Differential Pair Negative side;		SOC.E26
S81	no COEX & no BTRST	PCIE_C_TX+ / SERDES_1_TX+	MIPI_CSI1_D3_P	0	Available in SOM without "COEX" and without "BTRST" configuration; Differential Pair Positive side;		SOC.D26

8.3.1.3 MIPI CSI2 Signals – SMARC CSI1 pinout

Table 13: MIPI CSI2 Signals – SMARC CSI1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P3		CSI1_CK+	MIPI_CSI2_CLK_P	0			SOC.A23
P4		CSI1_CK-	MIPI_CSI2_CLK_N	0			SOC.B23
P7		CSI1_RX0+	MIPI_CSI2_D0_P	0	Differential Pair Positive side;		SOC.A25
P8		CSI1_RX0-	MIPI_CSI2_D0_N	0	Differential Pair Negative side;		SOC.B25
P10		CSI1_RX1+	MIPI_CSI2_D1_P	0	Differential Pair Positive side;		SOC.A24
P11		CSI1_RX1-	MIPI_CSI2_D1_N	0	Differential Pair Negative side;		SOC.B24
P13		CSI1_RX2+	MIPI_CSI2_D2_P	0	Differential Pair Positive side;		SOC.A22
P14		CSI1_RX2-	MIPI_CSI2_D2_N	0	Differential Pair Negative side;		SOC.B22
P16		CSI1_RX3+	MIPI_CSI2_D3_P	0	Differential Pair Positive side;		SOC.A21
P17		CSI1_RX3-	MIPI_CSI2_D3_N	0	Differential Pair Negative side;		SOC.B21
P109		GPIO1 / CAM1_PWR#	GPIO_EXP_P0_1__GPIO1_CAM1_PWR#	0	Signal source is GPIO Expander P0_1;	1.8V	PCAL6416 AHF,128.2

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P111		GPIO3 / CAM1_RST#	GPIO_EXP_P0_3__GPIO3_CAM1_RST#	0	Signal source is GPIO Expander P0_3;	1.8V	PCAL6416 AHF,128.4
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(I2C6_SCL)	3	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(I2C6_SDA)	3	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14

8.3.1.4   SMARC CSI0/1 Signals

Table 14: SMARC CSI0/1 Signals

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S6		CAM_MCK	GPIO1_IO15(CCM_CLKO2)	6		1.8V	SOC.B5

8.3.2   ISP

The Image Signal Processors (ISP) receive an image from the camera sensor and converts it from raw Bayer to YUV so it can be processed by the chip. The ISP also provides additional processing to improve the image quality. Supported image quality processes include:

- HDR to retain image details in high contrast scenes
- Dewarp to correct the image geometry caused by lens distortion (e.g. fisheye lens)
- Image enhancements (e.g. AWB, Denoise, AE, etc)

There are two instances of ISP on the chip and each is connected to separate instances of MIPI CSI. Both ISP instances support YCbCr420, YCbCR422, RAW8, RAW10, and RAW12 output pixel formats.

8.3.2.1   High-Dynamic Range (HDR)

The ISP supports the following HDR generation for high-quality on-the-fly dynamic range compression (DRC):

- Native HDR Sensor with compand output (max 14 bit compressed input)
- Digital Overlap High-Dynamic Range Sensor (DOL-HDR), staggered HDR For Native HDR sensors, the multi-exposure stitching is done internally and has line buffers.

Table 15: ISP0 & ISP1 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(ISP_FL_TRIG_0)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P43	WBE	SPI0_CS0#	GPIO1_IO00 (ISP_FL_TRIG_0)	3	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
P115		GPIO7	GPIO1_IO00 (ISP_FL_TRIG_0)	3	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
S57	QSPI	ESPI_IO_3 / QSPI_IO_3	NAND_DATA03(ISP_FL_TRIG_1)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.N24

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P114		GPIO6 / TACHIN	GPIO1_IO05 (ISP_FL_TRIG_1)	3		1.8V	SOC.B4
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(ISP_FLASH_TRIG_0)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
S145		WDT_TIME_OUT#	WDOG_B (ISP_FLASH_TRIG_0)	3		1.8V	SOC.B6
P118		GPIO10	GPIO1_IO07 (ISP_FLASH_TRIG_1)	3		1.8V	SOC.F6
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(ISP_PRELIGHT_TRIG_0)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25
P112		GPIO4 / HDA_RST#	GPIO1_IO03 (ISP_PRELIGHT_TRIG_0)	3		1.8V	SOC.D6
P37		SDIO_PWR_EN	GPIO1_IO08_3V3 (ISP_PRELIGHT_TRIG_1)	3	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(ISP_SHUTTER_OPEN_0)_QSPI_A_DQS	3		1.8V	SOC.R26
P6		GBE0_SDP	GPIO1_IO09(ISP_SHUTTER_OPEN_1)_3V3	3	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(ISP_SHUTTER_TRIG_0)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P117		GPIO9	GPIO1_IO01 (ISP_SHUTTER_TRIG_0)	3		1.8V	SOC.E8
S156	CHG	BATLOW#	GPIO1_IO06 (ISP_SHUTTER_TRIG_1)	3	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
P119		GPIO11	GPIO1_IO06 (ISP_SHUTTER_TRIG_1)	3	In SOM with "CHG" configuration, Duplicate pin on S156;	1.8V	SOC.A3

8.4 Ethernet Interface

The iMX 8M Plus implements Two Ethernet controllers both capable of simultaneous operation.

ENET_QOS (Ethernet Quality of Service) - Gigabit Ethernet controller based on Synopsys Proprietary with support for TSN (time-sensitive networking) in addition to EEE, Ethernet AVB, and IEEE 1588
ENET1 - Gigabit Ethernet controller with support for Energy Efficient Ethernet (EEE), Ethernet AVB (Audio Video Bridging, IEEE 802.1Qav), and IEEE 1588 time-stamping module which provides accurate clock synchronization for distributed control nodes for industrial automation applications.

The SOM can be ordered with up to x2 ETH PHYs assembled as described below:

- **"EC1" configuration** – The VAR-SMARC-MX8M-PLUS includes an on SOM a Gigabit PHY (TI P/N: DP83867IRRGZR) connected to ENET_QOS RGMII interface signals and exported on SMARC GBE0 pins. External connector and magnetics should be implemented on carrier board to complete the interface to the media.

- **"no EC" configuration** - The VAR-SMARC-MX8M-PLUS exposes the ENET_QOS RGMII/RMII interface signals to the SMARC 314-pin connector.

- **"EC2" configuration** – The VAR-SMARC-MX8M-PLUS includes an on SOM a Gigabit PHY (TI P/N: DP83867IRRGZR) connected to ENET1 interface signals and exported on SMARC GBE1 pins. External connector and magnetics should be implemented on carrier board to complete the interface to the media.

- **"no EC2" configuration** – ENET1 interface signals are not connected to an on SOM a Gigabit PHY, SMARC GBE1 pins are left Not Connected.

The on-SOM TI P/N: DP83867IRRGZR Gigabit PHYs in conjunction with external magnetics on carrier board complete the interface to the media.

The Following External Gigabit magnetics are recommended to complete the Ethernet PHY interface to the media.

Table 16: Gigabit Ethernet Magnetics

Vendor	P/N	Package	Cores	Configuration
Pulse	H5007NL	Transformer	8	Auto-MDX
TDK	TLA-7T101LF	Transformer	8	Auto-MDX
Pulse	J0G-0009NL	Integrated RJ45	8	Auto-MDX

8.4.1 Ethernet PHY EC1 Signals – SMARC GBE0 pinout

Table 17 Ethernet PHY EC1 Signals – SMARC GBE0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P28	EC1 & ETH_INT	GBE0_CTREF	ETH0_INT_IN	0	Signal source is Ethernet PHY EC1;	1.8V	GBE0_DP83867IRRGZ.44
P25	EC1	GBE0_LINK_ACT#	ETH0_LED_ACT	0	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.45 (Via inv. FET)
P22	EC1	GBE0_LINK_MAX#	ETH0_LED_LINK_1000	0	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.46 (Via inv. FET)
P21	EC1	GBE0_LINK_MID#	ETH0_LED_LINK_100	0	Signal source is Ethernet PHY EC1;	3.3V	GBE0_DP83867IRRGZ.39 (Via inv. FET)
P29	EC1	GBE0_MDI0-	ETH0_MDI_A_M	0	Signal source is Ethernet PHY EC1; Differential Pair Negative side;		GBE0_DP83867IRRGZ.2
P30	EC1	GBE0_MDI0+	ETH0_MDI_A_P	0	Signal source is Ethernet PHY EC1; Differential Pair Positive side;		GBE0_DP83867IRRGZ.1
P26	EC1	GBE0_MDI1-	ETH0_MDI_B_M	0	Signal source is Ethernet PHY EC1; Differential Pair Negative side;		GBE0_DP83867IRRGZ.5
P27	EC1	GBE0_MDI1+	ETH0_MDI_B_P	0	Signal source is Ethernet PHY EC1; Differential Pair Positive side;		GBE0_DP83867IRRGZ.4
P23	EC1	GBE0_MDI2-	ETH0_MDI_C_M	0	Signal source is Ethernet PHY EC1; Differential Pair Negative side;		GBE0_DP83867IRRGZ.8
P24	EC1	GBE0_MDI2+	ETH0_MDI_C_P	0	Signal source is Ethernet PHY EC1; Differential Pair Positive side;		GBE0_DP83867IRRGZ.7
P19	EC1	GBE0_MDI3-	ETH0_MDI_D_M	0	Signal source is Ethernet PHY EC1; Differential Pair Negative side;		GBE0_DP83867IRRGZ.11
P20	EC1	GBE0_MDI3+	ETH0_MDI_D_P	0	Signal source is Ethernet PHY EC1; Differential Pair Positive side;		GBE0_DP83867IRRGZ.10
P6		GBE0_SDP	GPIO1_IO09(ENET_QOS_1588_EVENT0_ OUT)_3V3	1	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)

8.4.2   Ethernet PHY EC2 Signals – SMARC GBE1 pinout

Table 18 Ethernet PHY EC2 Signals – SMARC GBE1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S28	EC2 & ETH_INT	GBE1_CTREF	ETH1_INT_IN	0	Signal source is Ethernet PHY EC2;	1.8V	GBE1_DP8 3867IRRG Z.44
S31	EC2	GBE1_LINK_ACT#	ETH1_LED_ACT	0	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP8 3867IRRG Z.45 (Via inv. FET)
S22	EC2	GBE1_LINK_MAX#	ETH1_LED_LINK_1000	0	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP8 3867IRRG Z.46 (Via inv. FET)
S19	EC2	GBE1_LINK_MID#	ETH1_LED_LINK_100	0	Signal source is Ethernet PHY EC2;	3.3V	GBE1_DP8 3867IRRG Z.39 (Via inv. FET)
S18	EC2	GBE1_MDI0-	ETH1_MDI_A_M	0	Signal source is Ethernet PHY EC2; Differential Pair Negative side;		GBE1_DP8 3867IRRG Z.2
S17	EC2	GBE1_MDI0+	ETH1_MDI_A_P	0	Signal source is Ethernet PHY EC2; Differential Pair Positive side;		GBE1_DP8 3867IRRG Z.1
S21	EC2	GBE1_MDI1-	ETH1_MDI_B_M	0	Signal source is Ethernet PHY EC2; Differential Pair Negative side;		GBE1_DP8 3867IRRG Z.5
S20	EC2	GBE1_MDI1+	ETH1_MDI_B_P	0	Signal source is Ethernet PHY EC2; Differential Pair Positive side;		GBE1_DP8 3867IRRG Z.4
S24	EC2	GBE1_MDI2-	ETH1_MDI_C_M	0	Signal source is Ethernet PHY EC2; Differential Pair Negative side;		GBE1_DP8 3867IRRG Z.8
S23	EC2	GBE1_MDI2+	ETH1_MDI_C_P	0	Signal source is Ethernet PHY EC2; Differential Pair Positive side;		GBE1_DP8 3867IRRG Z.7
S27	EC2	GBE1_MDI3-	ETH1_MDI_D_M	0	Signal source is Ethernet PHY EC2; Differential Pair Negative side;		GBE1_DP8 3867IRRG Z.11
S26	EC2	GBE1_MDI3+	ETH1_MDI_D_P	0	Signal source is Ethernet PHY EC2; Differential Pair Positive side;	1.8V	GBE1_DP8 3867IRRG Z.10
P5		GBE1_SDP	SAI1_RXC(ENET1_1588_EVENT0_OUT)_3V3	4	GBE1 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.AH8 (via push pull level shifter)

8.4.3 Ethernet PHY EC1/2 MDIO Signals – SMARC GBE0/1 MDIO pinout

Table 19 Ethernet PHY EC1/2 MDIO Signals – SMARC GBE0/1 MDIO pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S45		MDIO_CLK	ENET_QOS_MDC	0	GBE1/2 MDIO Clock Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V	SOC.AH28
S46		MDIO_DAT	ENET_QOS_MDIO	0	GBE1/2 MDIO Data Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V; PU 1.47K	SOC.AH29

8.4.4 ENET_QOS Signals - Proprietary SOM pinout (Non-SMARC)

Table 20: ENET_QOS RMII/RGMII Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P37		SDIO_PWR_EN	GPIO1_IO08_3V3 (ENET_QOS_1588_EVENT0_ AUX_IN)	4	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P37		SDIO_PWR_EN	GPIO1_IO08_3V3 (ENET_QOS_1588_EVENT0_ IN)	1	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P6		GBE0_SDP	GPIO1_IO09(ENET_QOS_1588_EVENT0_ OUT)_3V3	1	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)
P45		SPI0_DIN	I2C2_SCL(ENET_QOS_1588_EVENT1_ AUX_IN)	4		1.8V	SOC.AH6
P45		SPI0_DIN	I2C2_SCL(ENET_QOS_1588_EVENT1_ IN)	1		1.8V	SOC.AH6
P43	no WBE	SPI0_CS0#	I2C2_SDA(ENET_QOS_1588_EVENT1_ OUT)	1	Available in SOM without "WBE" configuration;	1.8V	SOC.AE8
S40		I2S0_SDOUT	SAI2_TXD(ENET_QOS_1588_EVENT2_ AUX_IN)	4		1.8V	SOC.AH16
S40		I2S0_SDOUT	SAI2_TXD(ENET_QOS_1588_EVENT2_ IN)	2		1.8V	SOC.AH16
S41		I2S0_SDIN	SAI2_RXD(ENET_QOS_1588_EVENT2_ OUT)	2		1.8V	SOC.AJ14
S38		AUDIO_MCK	SAI2_MCLK(ENET_QOS_1588_EVENT3_ AUX_IN)	4		1.8V	SOC.AJ15

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S38		AUDIO_MCK	SAI2_MCLK(ENET_QOS_1588_EVENT3_ IN)	2		1.8V	SOC.AJ15
S39		I2S0_LRCK	SAI2_TXFS(ENET_QOS_1588_EVENT3_ OUT)	2		1.8V	SOC.AJ17
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2 (ENET_QOS_INPUT=ENET_ QOS_TX_CLK OUTPUT=CCM_ENET_QOS_REF_ CLK_ROOT)	1	Available in SOM without "EC1" configuration; RMII clock - can be used in 2 schemes: • MAC generates output 50M reference clock for PHY, also MAC uses this 50M clock. • MAC uses external 50M clock.	1.8V	SOC.AF26
P44		SPI0_CK	I2C1_SCL(ENET_QOS_MDC)	1		1.8V	SOC.AC8
P119		GPIO11	GPIO1_IO06 (ENET_QOS_MDC)	1	In SOM with "CHG" configuration, Duplicate pin on S156;	1.8V	SOC.A3
S156	CHG	BATLOW#	GPIO1_IO06 (ENET_QOS_MDC)	1	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
P46		SPI0_DO	I2C1_SDA(ENET_QOS_MDIO)	1		1.8V	SOC.AH7
P118		GPIO10	GPIO1_IO07 (ENET_QOS_MDIO)	1		1.8V	SOC.F6
P24	no EC1	GBE0_MDI2+	ENET_QOS_RGMII_RD0	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AG29
P23	no EC1	GBE0_MDI2-	ENET_QOS_RGMII_RD1	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AG28
P20	no EC1	GBE0_MDI3+	ENET_QOS_RGMII_RD2	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AF29
P19	no EC1	GBE0_MDI3-	ENET_QOS_RGMII_RD3	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AF28
P25	no EC1	GBE0_LINK_ACT#	ENET_QOS_RGMII_RX_CTL	0	Available in SOM without "EC1" configuration; RGMII - Receive Control signal	1.8V	SOC.AE28
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC	0	Available in SOM without "EC1" configuration; RGMII - Receive Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @ 10Mbps Samples RD[3:0] and RX_CTL;	1.8V	SOC.AE29
P26	no EC1	GBE0_MDI1-	ENET_QOS_RGMII_TD0	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AC25
P27	no EC1	GBE0_MDI1+	ENET_QOS_RGMII_TD1	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AE26
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P30	no EC1	GBE0_MDI0+	ENET_QOS_RGMII_TD3	0	Available in SOM without "EC1" configuration;	1.8V	SOC.AD24
S54	no EC1	SATA_ACT#	ENET_QOS_RGMII_TX_CTL	0	Available in SOM without "EC1" configuration; RGMII - Transmit Control signal;	1.8V	SOC.AH13
P21	no EC1	GBE0_LINK_MID#	ENET_QOS_RGMII_TXC	0	Available in SOM without "EC1" configuration; RGMII - Transmit Clock: 125MHz @ 1000Mbps / 25MHz @ 100Mbps / 2.5MHz @	1.8V	SOC.AE24

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
					10Mbps Samples TD [3:0] and TX_CTL;		
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC (ENET_QOS_RX_ER)	1	Available in SOM without "EC1" configuration; RMII - RX_ER Signal	1.8V	SOC.AE29
P21	no EC1	GBE0_LINK_MID#	ENET_QOS_RGMII_TXC (ENET_QOS_TX_ER)	1	Available in SOM without "EC1" configuration; RMII - TX_ER signal;	1.8V	SOC.AE24

8.5   Wi-Fi & BT

The VAR-SMARC-MX8M-PLUS contains a certified high-performance Wi-Fi, Bluetooth, 802.15.4 module with the below features:
The VAR-SMARC-MX8M-PLUS module can be assembled with one of the following Wi-Fi modules:

- *"WBE"*
  Murata Type 2EL - 2.4GHz & 5GHz Wi-Fi® + Bluetooth® 5.4 BR/EDR/LE + 802.15.4 Module based on NXP IW612 chipset
- *"WBD"*
  Murata Type 2DL -2.4GHz & 5GHz Wi-Fi® + Bluetooth® 5.4 BR/EDR/LE Module based on NXP IW611 chipset
- *"WBK"*
  Murata Type 2KL - 2.4GHz & 5GHz Wi-Fi™ + Bluetooth® 5.4 Low Energy Module based on NXP IW610F chipset

All Modules have an antenna connection through a U. FL JACK connector
Antenna cable connected to module must have 50-Ω impedance

Figure 3 illustrates the VAR-SMARC-MX8M-PLUS internal Wi-Fi and BT connectivity.
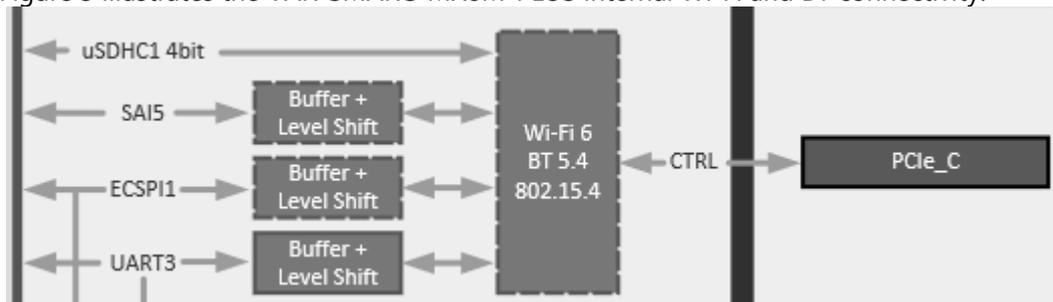
Figure 3: VAR-SMARC-MX8M-PLUS Wi-Fi & BT Internal Connection

NOTE

BT, 802.15.14, BT UART buffer, BT PCM buffer are controlled using GPIO2_IO11

- Logic "High" enables the BT, 802.15.14 and BT buffers.
- Logic "Low" disables them and releases the BT UART signals to be used via SOM connector.

802.15.4 buffer is controlled using GPIO5_IO17 (SPI0_CS0# signal)

- Logic "High" disables the buffer.
- Logic "Low" enables the buffer.

8.5.1　Interface Implementation Options

8.5.1.1　Module Configuration with "WBD" or "WBK" Option

- System use: **Wi-Fi and Bluetooth**.
  - BT UART external interface pins should be left floating.
- System use: **Wi-Fi and no BT**.
  - In this case, disable the BT buffers (using GPIO2_IO11) and BT function.
  - BT UART interface pins can be used externally with any of the alternate functions.
- System use: **BT and no Wi-Fi.**
  - Disable Wi-Fi function (using GPIO2_IO10)
  - Enable the BT buffer (using GPIO2_IO11) and BT function.

8.5.1.2　Module Configuration with "WBE" Option

- System use: **Wi-Fi and Bluetooth and 802.15.4**.
  - BT UART external interface pins should be left floating.
  - SPI0 interface pins can be used in SPI mode only
- System use: **Wi-Fi and no BT no 802.15.4**.
  - In this case, disable the BT and 802.15.4 module (using GPIO2_IO11) and 802.15.4 buffer (using GPIO5_IO17)
  - BT UART and SPI0 interface pins can be used externally with any of the alternate functions.
- System use: **BT and 802.15.4 and no Wi-Fi.**
  - Disable Wi-Fi function (using GPIO2_IO10).
  - Enable the BT and 802.15.4 module (using GPIO2_IO11).

8.5.1.3　Module Configuration without "WBD", "WBK", "WBE" Option

- System use: **no Wi-Fi and no BT**.
  - SPI0 and BT UART interface pin accessible externally with any of its alternative functions.

8.5.2　Bluetooth Interface Signals

Table 21: BT UART Interface Signals – SMARC SER2 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P136		SER2_TX	ECSPI1_MOSI(UART3_TX)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P137		SER2_RX	ECSPI1_SCLK(UART3_RX)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AF20
P138		SER2_RTS#	ECSPI1_MISO(UART3_CTS)	1	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT	1.8V	SOC.AD20

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
					Function disabled Always exposed		
P139		SER2_CTS#	ECSPI1_SS0(UART3_RTS)	1	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20

8.5.3   WLAN/BT Wake Interface signals

Note: WLAN/BT Wake signals are available on SOM with "WAKE" assembly option.

Table 22: WLAN/BT Host Wake signals

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S113	WAKE	eDP1_HPD / DSI1_TE	BT_DEV_WAKE_1V8	0	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2x L.75
S116	WAKE	LCD1_VDD_EN	BT_HOST_WAKE_1V8	0	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2x L.76
S107	WAKE	LCD1_BKLT_EN	WIFI_HOST_WAKE_1V8	0	Available in SOM with "WAKE" configuration;	1.8V	LBES5PL2x L.73

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

8.5.4   WIFI control signals - Proprietary SOM pinout (Non-SMARC)

Table 23: WIFI control Interface Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P80	COEX	PCIE_C_REFCK+	COEX_SIN_1V8	0	Available in SOM with "COEX" configuration;	1.8V	LBES5PL2x L.69
P81	COEX	PCIE_C_REFCK-	COEX_SOUT_1V8	0	Available in SOM with "COEX" configuration;	1.8V	LBES5PL2x L.70
S82	BTRST	PCIE_C_TX- / SERDES_1_TX-	BT_KILL_1V8	0	Available in SOM with "BTRST" configuration;	1.8V	LBES5PL2x L.64
S81	BTRST	PCIE_C_TX+ / SERDES_1_TX+	LR_KILL_1V8	0	Available in SOM with "BTRST" configuration;	1.8V	LBES5PL2x L.38
S77	WRST	PCIE_C_RST#	WB_KILL_1V8	0	Available in SOM with "WRST" configuration;	1.8V	LBES5PL2x L.63

Note: These assembly options were not fully tested yet; for further support, please contact sales@variscite.com

8.6 Ultra-Secured Digital Host Controller

8.6.1 uSDHC1 Signals

uSDHC controller, uSDHC1, is used internally for the Wi-Fi SDIO interface on the SOM.

8.6.2 uSDHC2 Signals – SMARC SDIO pinout

The VAR-SMARC-MX8M-PLUS exposes the i.MX8M-PLUS uSDHC2 controller 4-bit interface for supporting interface between the host system and the SD/SDIO/MMC cards to the SMARC SDIO pins.

Key features of uSDHC2:

- SD/SDIO standard, up to version 3.0.
- MMC standard, up to version 5.1.
- 1.8 V and 3.3 V operation
- 1-bit/4-bit SD and SDIO modes, 1-bit/4-bit MMC mode
- Up to SDR104 rate

The SMARC specification defines 1x SDIO interface which is mapped to the i.MX8M-PLUS uSDHC2 interface.

Table 24: uSDHC2 Signals – SMARC SDIO pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P33		SDIO_WP	SD2_WP(USDHC2_WP)	0		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AC26
P34		SDIO_CMD	SD2_CMD(USDHC2_CMD)	0		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AB28
P35		SDIO_CD#	SD2_CD_B(USDHC2_CD_B)	0		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AD29
P36		SDIO_CK	SD2_CLK(USDHC2_CLK)	0		Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
P37		SDIO_PWR_EN	GPIO1_IO08_3V3	0	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P39		SDIO_D0	SD2_DATA0(USDHC2_DATA0)	0		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
P40		SDIO_D1	SD2_DATA1(USDHC2_DATA1)	0		Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
P41		SDIO_D2	SD2_DATA2(USDHC2_DATA2)	0		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
P42		SDIO_D3	SD2_DATA3(USDHC2_DATA3)	0		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25

8.6.3   uSDHC3 Signals

uSDHC controller, uSDHC3, is used internally for the eMMC interface on the SOM.

8.7   USB

The VAR-SMARC-MX8M-PLUS exports the two i.MX8M-PLUS USB2.0/3.0 ports to the SOM's pins according to the SMARC specification sections 3.14.1, 3.14.2.

The i.MX8M-PLUS SoC USB1 port is routed directly to SMARC USB0 Port.
The MX8M-PLUS SoC USB2 port can be routed to TI's USB HUB P/N: TUSB8041IRGCR
 (**"HUB" configuration**) providing additional USB ports or bypassed and routed directly to SMARC USB2 Port (**"no HUB" configuration**).

Figure *3*4 illustrates the VAR-SMARC-MX8M-PLUS USB connectivity scheme:
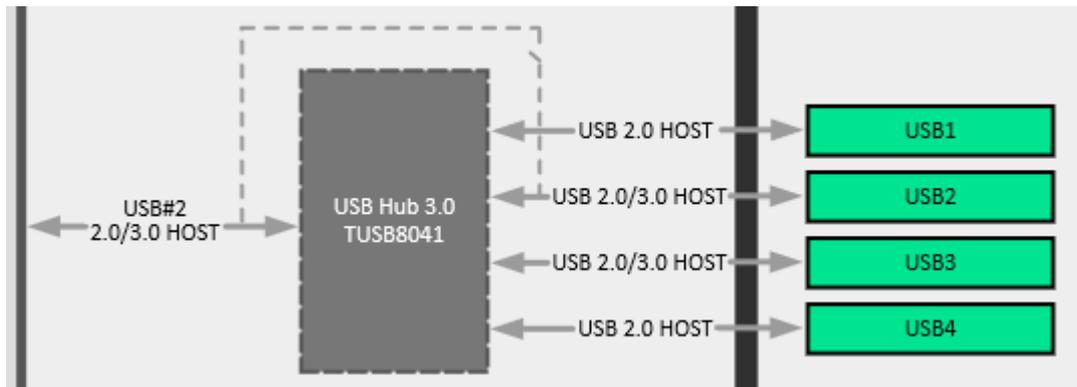
Figure 4: VAR-SMARC-MX8M-PLUS USB Connection

The SMARC specification defines up to x5 USB ports, depending on SOM configuration, the below SMARC USB ports are possible:

Table 25: SMARC USB port options

SMARC USB Port#	With "HUB"	Without "HUB"
USB0	SoC USB1 2.0 - OTG	SoC USB1 2.0 - OTG
USB1	HUB Port#1 USB 2.0 - HOST	N/A
USB2	HUB Port#2 USB 2.0 /3.0 - HOST	SoC USB2 2.0 /3.0 - HOST
USB3	HUB Port#3 USB 2.0 /3.0 - HOST	N/A
USB4	HUB Port#4 USB 2.0 - HOST	N/A
USB5	N/A	N/A

8.7.1 USB1 Signals - SMARC USB Port0 pinout

Table 26: USB1 Signals - SMARC USB Port0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P60		USB0+	USB1_DP	0	Soc USB1 - USB0 2.0 - OTG; Differential Pair Positive side		P60
P61		USB0-	USB1_DN	0	Soc USB1 - USB0 2.0 - OTG; Differential Pair Negative side		P61
P62		USB0_EN_OC#	GPIO1_IO13_3V3	0	SoC USB1 - USB0 Over-Current Sense GPIO;	3.3V, via bidirectional OD level shifter; with 10K PU	P62
P63		USB0_VBUS_DET	USB1_VBUS	0	Soc USB1 - USB0 VBUS;	5V	P63
P64		USB0_OTG_ID	GPIO1_IO10(GPIO1_IO10)_3V3	0	SoC USB1 - USB0_OTG_ID GPIO;	3.3V, Input via push pull level shifter	P64

8.7.2 USB2 Signals - SMARC USB Port1 pinout (via HUB)

Table 27: USB2 Signals - SMARC USB Port1 pinout (via HUB)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P65	HUB	USB1+	USBH_P1_DP	0	Available in SOM with "HUB" configuration; USB1 - USB 2.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.1
P66	HUB	USB1-	USBH_P1_DN	0	Available in SOM with "HUB" configuration; USB1 - USB 2.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.2
P67	HUB	USB1_EN_OC#	P1_EN_OC_N_3V3	0	Available in SOM with "HUB" configuration; USB1 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041 IRGCR.46

8.7.3 USB2 Signals - SMARC USB Port2 pinout (via HUB)

Table 28: USB2 Signals - SMARC USB Port2 pinout (via HUB)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P69	HUB	USB2+	USBH_P2_DP	0	Available in SOM with "HUB" configuration; USB2 - USB 2.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.9
P70	HUB	USB2-	USBH_P2_DN	0	Available in SOM with "HUB" configuration; USB2 - USB 2.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.10

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P71	HUB	USB2_EN_OC#	P2_EN_OC_N_3V3	0	Available in SOM with "HUB" configuration; USB2 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041 IRGCR.47
S71	HUB	USB2_SSTX+	USBH_P2_C_SSTXP	0	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.11
S72	HUB	USB2_SSTX-	USBH_P2_C_SSTXN	0	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.12
S74	HUB	USB2_SSRX+	USBH_P2_SSRXP	0	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.14
S75	HUB	USB2_SSRX-	USBH_P2_SSRXN	0	Available in SOM with "HUB" configuration; USB2 - USB 3.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.15

8.7.4 USB2 Signals - SMARC USB Port2 pinout (no HUB)

Table 29: USB2 Signals - SMARC USB Port2 pinout (no HUB))

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P69	no HUB	USB2+	USB2_D_P	0	Available in SOM without "HUB" configuration; SoC USB2 2.0 signal; Differential Pair Positive side;		SOC.D14
P70	no HUB	USB2-	USB2_D_N	0	Available in SOM without "HUB" configuration; SoC USB2 2.0 signal Differential Pair Negative side;		SOC.E14
P71	no HUB	USB2_EN_OC#	GPIO_EXP_P1_2__P2_EN_OC_N_3V3	0	Available in SOM without "HUB configuration; USB2 Enable/Over-Current Sense; Signal source is GPIO Expander P1_2;	3.3V via bidirectional OD level shifter with 10K PU	PCAL6416 AHF,128.12 (via bidirectional OD level shifter)
S71	no HUB	USB2_SSTX+	USB2_TX_P	0	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal; Differential Pair Positive side;		SOC.A13
S72	no HUB	USB2_SSTX-	USB2_TX_N	0	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal; Differential Pair Negative side;		SOC.B13
S74	no HUB	USB2_SSRX+	USB2_RX_P	0	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal; Differential Pair Positive side;		SOC.A12
S75	no HUB	USB2_SSRX-	USB2_RX_N	0	Available in SOM without "HUB" configuration; SoC USB2 3.0 signal; Differential Pair Negative side;		SOC.B12

8.7.5   USB2 Signals – SMARC USB Port3 pinout (via HUB)

Table 30: USB2 Signals - SMARC USB Port3 pinout (via HUB)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P74	HUB	USB3_EN_OC#	P3_EN_OC_N_3V3	0	Available in SOM with "HUB" configuration; USB3 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041 IRGCR.44
S62	HUB	USB3_SSTX+	USBH_P3_C_SSTXP	0	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.19
S63	HUB	USB3_SSTX-	USBH_P3_C_SSTXN	0	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.20
S65	HUB	USB3_SSRX+	USBH_P3_SSRXP	0	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.22
S66	HUB	USB3_SSRX-	USBH_P3_SSRXN	0	Available in SOM with "HUB" configuration; USB3 - USB 3.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.23
S68	HUB	USB3+	USBH_P3_DP	0	Available in SOM with "HUB" configuration; USB3 - USB 2.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.17
S69	HUB	USB3-	USBH_P3_DN	0	Available in SOM with "HUB" configuration; USB3 - USB 2.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.18

8.7.6   USB2 Signals – SMARC USB Port4 pinout (via HUB)

Table 31: USB2 Signals - SMARC USB Port4 pinout (via HUB)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P76	HUB	USB4_EN_OC#	P4_EN_OC_N_3V3	0	Available in SOM with "HUB" configuration; USB4 - Over-Current Sense via HUB;	3.3V; PU 10K	TUSB8041 IRGCR.43
S35	HUB	USB4+	USBH_P4_DP	0	Available in SOM with "HUB" configuration; USB4 - USB 2.0 HOST via HUB; Differential Pair Positive side;		TUSB8041 IRGCR.24
S36	HUB	USB4-	USBH_P4_DN	0	Available in SOM with "HUB" configuration; USB4 - USB 2.0 HOST via HUB; Differential Pair Negative side;		TUSB8041 IRGCR.25

8.7.7   USB2 Interface Signals – Proprietary SOM pinout (Non-SMARC)

The VAR-SMARC-MX8M-PLUS also exposes the i.MX8M-PLUS SoC USB2 Interface pins, which can be optionally used in **"no HUB"** configuration.

Table 32: USB2 Interface Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S6		CAM_MCK	GPIO1_IO15(USB2_OTG_OC)	1		1.8V	SOC.B5
P113		GPIO5 / PWM_OUT	GPIO1_IO14(USB2_OTG_PWR)	1		1.8V	SOC.A4

8.8   PCIe

The VAR-SMARC-MX8M-PLUS exposes a single PCI Express Gen 3.0 single lane interface.
The PCI Express port requires an external 100MHz PCIe compliant reference clock if the function is enabled.

On the VAR-SMARC-MX8M-PLUS, a PCIE clock generator chip (Microchip P/N: DSC557-0344FL1T) is used to feed high-quality clock to both the internal SoC PHY and an external connecter/device.

The PCIe controller implements the following standards:
- PCI Express Base Specification, Revision 4.0, Version 0.7
- PCI Local Bus Specification, Revision 3.0
- PCI Bus Power Management Specification, Revision 1.2
- PCI Express Card Electromechanical Specification, Revision 1.1

Note: Access to the above specification requires membership in PCI-SIG.

The following lists the key features of the Samsung PCIe PHY IP core used for PCI-Express (PCIe) applications:

- 2.5Gb/s, 5.0Gb/s, and 8.0Gb/s Serializer/De-serializer
- Serializes the 8b/10b encoded data for transmission for Gen1 and Gen2 operation, and 128b/130b encoded data for Gen3. De-serializes the received code groups
- PHY Interface for the PCI Express Architecture, Version 4.2 compliance
- Spread Spectrum Clocking in Transmitter and Receiver
- Separate Refclk Independent SSC (SRIS) Architecture
- Continuous-Time Linear Equalizer and 5-tap adaptive Decision-Feedback Equalizer

The SMARC specification defines up to 4x DSI display interfaces, 1x of which can be achieved through the i.MX 8M Plus SoC PCIE interface.

8.8.1   PCIE Signals – SMARC PCIE_A pinout

Table 33: PCIE Signals – SMARC PCIE_A pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P75		PCIE_A_RST#	GPIO_EXP_P1_6__PCIE_A_RST#_3V3	0	Signal source is GPIO Expander P1_6;	3.3V, via bidirectional OD level shifter; with 10k PU	PCAL6416AHF,128.16 (via bidirectional OD level shifter)
P78		PCIE_A_CKREQ#	PCIE_A_CKREQ#	0	Input signal to on SOM clock generator;	3.3V; PU 20K	DSC557-0344FL1T.1 (Via inv. FET)
P83		PCIE_A_REFCK+	PCIE_A_REFCK+	0	Signal Source is on SOM clock generator; Differential Pair Positive side;		DSC557-0344FL1T.8

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P84		PCIE_A_REFCK-	PCIE_A_REFCK-	0	Signal Source is on SOM clock generator; Differential Pair Negative side;		DSC557-0344FL1T.9
P86		PCIE_A_RX+	PCIE_RXN_P	0	Differential Pair Positive side;		SOC.A14
P87		PCIE_A_RX-	PCIE_RXN_N	0	Differential Pair Negative side;		SOC.B14
P89		PCIE_A_TX+	PCIE_TXN_P	0	Differential Pair Positive side;		SOC.A15
P90		PCIE_A_TX-	PCIE_TXN_N	0	Differential Pair Negative side;		SOC.B15

8.9 Audio

The following audio interfaces are available with the VAR-SMARC-MX8M-PLUS:

- WM8904CGEFL Audio codec interfaces:
    - o Analog outputs & inputs: stereo line-in & Stereo HP out.
    - o Digital microphone input
- Up to 6 external SAI (synchronous audio interface) modules supporting I2S, AC97, TDM, codec/DSP and DSD interfaces:
- PDM supporting up to 8-channels (4 lanes)
- S/PDIF Input and Output, including a new Raw Capture input mode
- Hifi4 Audio DSP, operating up to 800 MHz

The SMARC specification defines 2x I2S interfaces: I2S0, I2S2.
SMARC I2S0 is mapped to the SoC SAI2 signals and exported on SMARC I2S0 pins.
SMARC I2S2 -
- with **"AC"** Configuration - SoC SAI3 signals are connected on SOM WM8904 audio codec. The Analog codec interface pins are exported on SMARC I2S2 pins
- with **"no AC"-** SoC SAI3 signals are exported to SMARC I2S2 pins

8.9.1 WM8904CGEFL Audio Codec

The Codec features stereo ground-referenced headphone amplifiers using the Wolfson 'Class-W' amplifier techniques -incorporating an innovative dual-mode charge pump architecture - to optimize efficiency and power consumption during playback. The ground-referenced headphone and line outputs eliminate AC coupling capacitors, and both outputs include common mode feedback paths to reject ground noise.

The following figure illustrates the connectivity for no large AC coupling capacitors implemented on SOM.
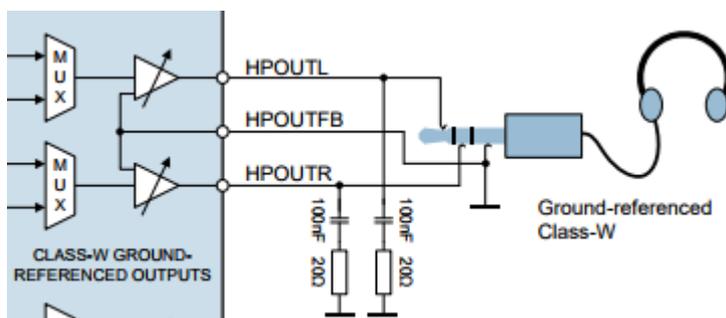
Figure 5: WM8904 Headphone connectivity

8.9.1.1 Audio Codec Signals – Proprietary SOM pinout (Non-SMARC)

Table 34: Analog audio Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P50	AC	GND	AGND	0	Signal source is Audio Codec;		AGND
S43	AC	ESPI_ALERT0#	DMIC_CLK	0	Signal source is Audio Codec;	1.8V	WM8904.1
S44	AC	ESPI_ALERT1#	DMIC_DATA	0	Signal source is Audio Codec;	1.8V	WM8904.27
S52	AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	HPLOUT	0	Signal source is Audio Codec;		WM8904.13
S53	AC	I2S2_CK / HDA_CK / SNDW_CLK0	HPROUT	0	Signal source is Audio Codec;		WM8904.15
S51	AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	LINEIN1_LP	0	Signal source is Audio Codec;		WM8904.26
S50	AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	LINEIN1_RP	0	Signal source is Audio Codec;		WM8904.24
S58	AC	ESPI_RESET#	HPOUTFB	0	Signal source is Audio Codec;		WM8904.14

8.9.2 Serial Audio Interface

The SAI module provides a synchronous audio interface that supports full duplex serial interfaces with frame synchronization, such as I2S, AC97, TDM, and codec/DSP interfaces.

The following table details the SAI interface signals definition.

Table 35: SAI interface signals definition

Name	Function	DIR
SAI_TXC	Transmit Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_TXFS	Transmit Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_TXD	Transmit Data. The transmit data is generated synchronously by the bit clock and is tristate whenever not transmitting a word	O
SAI_RXC	Receive Bit Clock. The bit clock is an input when externally generated and an output when internally generated.	I/O
SAI_RXFS	Receive Frame Sync. The frame sync is an input sampled synchronously by the bit clock when externally generated and an output generated synchronously by the bit clock when internally generated.	I/O
SAI_RXD	Receive Data. The receive data is sampled synchronously by the bit clock.	I

8.9.2.1   SAI1 Signals– Proprietary SOM pinout (Non-SMARC)

Table 36: SAI1 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P31		SPI0_CS1#	SAI1_MCLK(SAI1_MCLK)	0		1.8V	SOC.AE12
P5		GBE1_SDP	SAI1_RXC(SAI1_RX_BCLK)_3V3	0	GBE1 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.AH8 (via push pull level shifter)
P116		GPIO8	SAI1_RXD0(SAI1_RX_DATA0)	0		1.8V	SOC.AC10
S149		SLEEP#	SAI1_RXFS(SAI1_RX_SYNC)	0		1.8V; PU 10K	SOC.AJ9
P31		SPI0_CS1#	SAI1_MCLK(SAI1_TX_BCLK)	2		1.8V	SOC.AE12
P146		CAN1_RX	SAI5_MCLK(SAI1_TX_BCLK)	1		1.8V	SOC.AF14
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(SAI1_TX_DATA0)	1	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S139		I2C_LCD_CK	SAI5_RXFS(SAI1_TX_DATA0)	1	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
P116		GPIO8	SAI1_RXD0(SAI1_TX_DATA1)	2		1.8V	SOC.AC10
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(SAI1_TX_DATA1)	1	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S140		I2C_LCD_DAT	SAI5_RXC(SAI1_TX_DATA1)	1	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
S148		LID#	SAI1_TXD6(SAI1_TX_DATA6)	0		1.8V; PU 10K	SOC.AC12
P1		SMB_ALERT#	SAI1_TXD7(SAI1_TX_DATA7)	0		1.8V; PU 2.2K	SOC.AJ13

8.9.2.2   SAI2 Signals - SMARC I2S0 pinout

Table 37: SAI2 Signals - SMARC I2S0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S38		AUDIO_MCK	SAI2_MCLK(SAI2_MCLK)	0		1.8V	SOC.AJ15
S39		I2S0_LRCK	SAI2_TXFS(SAI2_TX_SYNC)	0		1.8V	SOC.AJ17
S39		I2S0_LRCK	SAI2_TXFS(SAI2_TX_DATA1)	3		1.8V	SOC.AJ17
S40		I2S0_SDOUT	SAI2_TXD(SAI2_TX_DATA0)	0		1.8V	SOC.AH16
S41		I2S0_SDIN	SAI2_RXD(SAI2_RX_DATA0)	0		1.8V	SOC.AJ14
S41		I2S0_SDIN	SAI2_RXD(SAI2_TX_DATA1)	3		1.8V	SOC.AJ14
S42		I2S0_CK	SAI2_TXC(SAI2_TX_BCLK)	0		1.8V	SOC.AH15

8.9.2.3   SAI2 Signals – Proprietary SOM pinout (Non-SMARC)

Table 38: SAI2 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S142		GPIO12	SAI2_RXC(SAI2_RX_BCLK)	0	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(SAI2_RX_BCLK)	0	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SAI2_RX_DATA1)	1	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S123		GPIO13	SAI2_RXFS(SAI2_RX_DATA1)	3	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17
S151	CHG	CHARGING#	SAI2_RXFS(SAI2_RX_DATA1)	3	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(SAI2_RX_DATA2)	1	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(SAI2_RX_DATA3)	1	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S123		GPIO13	SAI2_RXFS(SAI2_RX_SYNC)	0	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17
S151	CHG	CHARGING#	SAI2_RXFS(SAI2_RX_SYNC)	0	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(SAI2_TX_DATA1)	1	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(SAI2_TX_DATA2)	1	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SAI2_TX_DATA3)	1	Available in SOM without "AC" configuration;	1.8V	SOC.AH18

8.9.2.4 SAI3 Signals - SMARC I2S2 pinout

Note: SAI3 interface is used by internal Audio Codec.
SAI3 interface can be used externally only in SOMs without "AC" assembly option.

Table 39: SAI3 Signals - SMARC I2S2 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(SAI3_TX_SYNC)	0	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SAI3_TX_DATA0)	0	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(SAI3_RX_DATA0)	0	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(SAI3_TX_BCLK)	0	Available in SOM without "AC" configuration;	1.8V	SOC.AH19

8.9.2.5 SAI3 Signals - Proprietary SOM pinout (Non-SMARC)

Note: SAI3 interface is used by internal Audio Codec.
SAI3 interface can be used externally only in SOMs without "AC" assembly option.
Some signals are available on SOM with "SAI3" assembly option.

Table 40: SAI3 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(SAI3_MCLK)_QSPI_A_DQS	2		1.8V	SOC.R26
S38		AUDIO_MCK	SAI2_MCLK(SAI3_MCLK)	6		1.8V	SOC.AJ15
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (SAI3_MCLK)	0	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(SAI3_RX_BCLK)	0	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(SAI3_RX_DATA0)	2	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(SAI3_RX_DATA0)	0	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SAI3_RX_DATA1)	3	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SAI3_RX_SYNC)	0	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(SAI3_TX_BCLK)	2	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(SAI3_TX_DATA0)	2	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(SAI3_TX_SYNC)	2	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25

8.9.2.6 SAI5 Signals – Proprietary SOM pinout (Non-SMARC)

Table 41: SAI5 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P146		CAN1_RX	SAI5_MCLK(SAI5_MCLK)	0		1.8V	SOC.AF14
S38		AUDIO_MCK	SAI2_MCLK(SAI5_MCLK)	1		1.8V	SOC.AJ15
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (SAI5_MCLK)	2	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(SAI5_RX_BCLK)	0	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(SAI5_RX_BCLK)	2	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
S140		I2C_LCD_DAT	SAI5_RXC(SAI5_RX_BCLK)	0	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(SAI5_RX_DATA0)	2	Available in SOM without "AC" configuration;	1.8V	SOC.AF18

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(SAI5_RX_DATA1)	2	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(SAI5_RX_DATA2)	2	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SAI5_RX_DATA3)	2	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(SAI5_RX_SYNC)	0	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SAI5_RX_SYNC)	2	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S139		I2C_LCD_CK	SAI5_RXFS(SAI5_RX_SYNC)	0	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
S142		GPIO12	SAI2_RXC(SAI5_TX_BCLK)	1	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(SAI5_TX_BCLK)	1	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
S41		I2S0_SDIN	SAI2_RXD(SAI5_TX_DATA0)	1		1.8V	SOC.AJ14
S39		I2S0_LRCK	SAI2_TXFS(SAI5_TX_DATA1)	1		1.8V	SOC.AJ17
S123		GPIO13	SAI2_RXFS(SAI5_TX_DATA1)	2	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17
S151	CHG	CHARGING#	SAI2_RXFS(SAI5_TX_DATA1)	2	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17

8.9.2.7 SAI6 Signals – Proprietary SOM pinout (Non-SMARC)

Table 42: SAI6 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P1		SMB_ALERT#	SAI1_TXD7(SAI6_MCLK)	1		1.8V; PU 2.2K	SOC.AJ13
S54	no EC1	SATA_ACT#	ENET_QOS_RGMII_TX_CTL (SAI6_MCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AH13
P26	no EC1	GBE0_MDI1-	ENET_QOS_RGMII_TD0 (SAI6_RX_BCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AC25
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2 (SAI6_RX_DATA0)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P27	no EC1	GBE0_MDI1+	ENET_QOS_RGMII_TD1 (SAI6_RX_SYNC)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AE26
S148		LID#	SAI1_TXD6(SAI6_RX_SYNC)	1		1.8V; PU 10K	SOC.AC12
P30	no EC1	GBE0_MDI0+	ENET_QOS_RGMII_TD3 (SAI6_TX_BCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AD24
S45		MDIO_CLK	ENET_QOS_MDC (SAI6_TX_DATA0)	2	GBE1/2 MDIO Clock Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V	SOC.AH28
S46		MDIO_DAT	ENET_QOS_MDIO (SAI6_TX_SYNC)	2	GBE1/2 MDIO Data Signal; Pin alternate function cannot be changed when using SOM with EC assembled	1.8V; PU 1.47K	SOC.AH29

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
					Do not alter pinmux with "EC1" or "EC2" configuration		
S148		LID#	SAI1_TXD6(SAI6_TX_SYNC)	2		1.8V; PU 10K	SOC.AC12

8.9.2.8 SAI7 Signals – Proprietary SOM pinout (Non-SMARC)

Table 43: SAI7 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P19	no EC1	GBE0_MDI3-	ENET_QOS_RGMII_RD3 (SAI7_MCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AF28
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (SAI7_MCLK)	3	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
P20	no EC1	GBE0_MDI3+	ENET_QOS_RGMII_RD2 (SAI7_RX_BCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AF29
P136		SER2_TX	ECSPI1_MOSI(SAI7_RX_BCLK)	3	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P24	no EC1	GBE0_MDI2+	ENET_QOS_RGMII_RD0 (SAI7_RX_DATA0)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AG29
P138		SER2_RTS#	ECSPI1_MISO(SAI7_RX_DATA0)	3	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P23	no EC1	GBE0_MDI2-	ENET_QOS_RGMII_RD1 (SAI7_RX_SYNC)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AG28
P137		SER2_RX	ECSPI1_SCLK(SAI7_RX_SYNC)	3	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AF20
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC (SAI7_TX_BCLK)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AE29
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK (SAI7_TX_BCLK)	3	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P21	no EC1	GBE0_LINK_MID#	ENET_QOS_RGMII_TXC (SAI7_TX_DATA0)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AE24
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI (SAI7_TX_DATA0)	3	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21
P25	no EC1	GBE0_LINK_ACT#	ENET_QOS_RGMII_RX_CTL (SAI7_TX_SYNC)	2	Available in SOM without "EC1" configuration;	1.8V	SOC.AE28
P139		SER2_CTS#	ECSPI1_SS0(SAI7_TX_SYNC)	3	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20

8.9.3 PDM - Microphone Interface (MICFIL)

The PDM module of the i.MX 8M Plus SOC, provides a popular way to deliver audio from microphones to the processor in several applications, such as mobile telephones.
Up to 8 channels can be implemented with 4 lanes.

The PDM Microphone Interface module is composed of:
- An input interface for each pair of PDM microphones.
- A decimation filter by channel.
- A FIFO by channel.
- A time generation unit.
- Shared interfaces to DMA, interrupts and SoC.
- One or more Hardware Voice Activity Detectors (HWVAD).

PDM block main features are:
- Decimation filters:
  o Fixed filtering characteristics for audio application.
  o 24-bit signed filter output.
  o Maximum dynamic range: 120dB.
  o Internal clock divider for a programmable PDM clock generation.
  o Full or partial set of channels operation with individual enable control.
  o Programmable decimation rate.
  o Programmable DC remover.
  o Range adjustment capability.
  o FIFOs with interrupt and DMA capability.
    ▪ Each FIFO with 32 entries length.
- Hardware Voice Activity Detector (HWVAD).
  o Interrupt capability.
  o Zero-Crossing Detection (ZCD) option.

Table 44: PDM Interface Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P23	no EC1	GBE0_MDI2-	ENET_QOS_RGMII_RD1 (PDM_BIT_STREAM0)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AG28
P27	no EC1	GBE0_MDI1+	ENET_QOS_RGMII_TD1 (PDM_BIT_STREAM0)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AE26
P39		SDIO_D0	SD2_DATA0(PDM_BIT_STREAM0)	4		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
P116		GPIO8	SAI1_RXD0(PDM_BIT_STREAM0)	3		1.8V	SOC.AC10
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(PDM_BIT_STREAM0)	6	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
P24	no EC1	GBE0_MDI2+	ENET_QOS_RGMII_RD0 (PDM_BIT_STREAM1)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AG29
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2 (PDM_BIT_STREAM1)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P40		SDIO_D1	SD2_DATA1(PDM_BIT_STREAM1)	4		Bank voltage set on	SOC.AC29

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
						SOM 1.8V/3.3V	
S42		I2S0_CK	SAI2_TXC(PDM_BIT_STREAM1)	6		1.8V	SOC.AH15
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(PDM_BIT_STREAM1)	6	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S142		GPIO12	SAI2_RXC(PDM_BIT_STREAM1)	6	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(PDM_BIT_STREAM1)	6	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC (PDM_BIT_STREAM2)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AE29
P30	no EC1	GBE0_MDI0+	ENET_QOS_RGMII_TD3 (PDM_BIT_STREAM2)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AD24
P41		SDIO_D2	SD2_DATA2(PDM_BIT_STREAM2)	4		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
S39		I2S0_LRCK	SAI2_TXFS(PDM_BIT_STREAM2)	6		1.8V	SOC.AJ17
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(PDM_BIT_STREAM2)	6	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
P25	no EC1	GBE0_LINK_ACT#	ENET_QOS_RGMII_RX_CTL (PDM_BIT_STREAM3)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AE28
P42		SDIO_D3	SD2_DATA3(PDM_BIT_STREAM3)	4		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
S41		I2S0_SDIN	SAI2_RXD(PDM_BIT_STREAM3)	6		1.8V	SOC.AJ14
S46		MDIO_DAT	ENET_QOS_MDIO (PDM_BIT_STREAM3)	3	GBE1/2 MDIO Data Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V; PU 1.47K	SOC.AH29
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(PDM_BIT_STREAM3)	6	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S123		GPIO13	SAI2_RXFS(PDM_BIT_STREAM3)	6	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17
S151	CHG	CHARGING#	SAI2_RXFS(PDM_BIT_STREAM3)	6	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
P1		SMB_ALERT#	SAI1_TXD7(PDM_CLK)	3		1.8V; PU 2.2K	SOC.AJ13
P5		GBE1_SDP	SAI1_RXC(PDM_CLK)_3V3	3	GBE1 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.AH8 (via push pull level shifter)
P20	no EC1	GBE0_MDI3+	ENET_QOS_RGMII_RD2 (PDM_CLK)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AF29
P26	no EC1	GBE0_MDI1-	ENET_QOS_RGMII_TD0 (PDM_CLK)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AC25
P34		SDIO_CMD	SD2_CMD(PDM_CLK)	4		Bank voltage set on	SOC.AB28

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
						SOM 1.8V/3.3V; PU 10K	
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(PDM_CLK)	4	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(PDM_CLK)	6	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
S140		I2C_LCD_DAT	SAI5_RXC(PDM_CLK)	4	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14

8.9.4   SPDIF – Sony Philips Digital Interface Format

A standard audio file transfer format, developed jointly by the Sony and Phillips corporations. It supports Transmitter and Receiver functionality including frequency measurement block that allows the precise measurement of an incoming sampling frequency.
The SPDIF receiver extracts the audio data from each SPDIF frame and places the data in the SPDIF Rx left and right FIFOs with Channel Status and User bits.
For the SPDIF transmitter, the audio data is provided by the processor dedicated registers along with Channel Status and User bits.

Table 45: SPDIF Interface Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SPDIF1_EXT_CLK)	4	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(SPDIF1_EXT_CLK)	0		1.8V	SOC.AC18
P19	no EC1	GBE0_MDI3-	ENET_QOS_RGMII_RD3 (SPDIF1_IN)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AF28
P42		SDIO_D3	SD2_DATA3(SPDIF1_IN)	3		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
P144		CAN0_RX	SPDIF_RX(SPDIF1_IN)	0		1.8V	SOC.AD18
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(SPDIF1_IN)	4	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (SPDIF1_IN)	6	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
P41		SDIO_D2	SD2_DATA2(SPDIF1_OUT)	3		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
P143		CAN0_TX	SPDIF_TX(SPDIF1_OUT)	0		1.8V	SOC.AE18
S54	no EC1	SATA_ACT#	ENET_QOS_RGMII_TX_CTL (SPDIF1_OUT)	3	Available in SOM without "EC1" configuration;	1.8V	SOC.AH13
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (SPDIF1_OUT)	4	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20

8.10 UART

The VAR-SMARC-MX8M-PLUS exposes the 4x i.MX8M-PLUS UART interfaces.

The SMARC specification defines 4x UART interfaces SER0/1/2/3. Ports SER0 and SER2 are 4 wire ports (2 data lines and 2 handshake lines). Ports SER1 and SER3 are 2 wire ports (data only). SER0/1/2/3 are mapped to the i.MX8M-PLUS UART1/2/3/4 respectively.

SMARC SER2 Port exported by UART3 is used on SOM for Bluetooth interface and can be accessible only if the on-SOM buffer is disabled or on SOM without **"WBD", "WBK", "WBE" Configuration**.

The UART includes the following features:
- High-speed TIA/EIA-232-F compatible, up to 5 Mbit/s
- Serial IR interface low-speed, IrDA-compatible (up to 115.2 Kbit/s)
- 9-bit or Multidrop mode (RS-485) support (automatic slave address detection)
- 7 or 8 data bits for RS-232 characters, or 9 bit RS-485 format
- 1 or 2 stop bits
- Programmable parity (even, odd, and no parity)
- Hardware flow control support for request to send (RTS_B) and clear to send (CTS_B) signals
- RS-485 driver direction control via CTS_B signal
- Edge-selectable RTS_B and edge-detect interrupts
- Status flags for various flow control and FIFO states
- Voting logic for improved noise immunity (16x oversampling)
- Transmitter FIFO empty interrupt suppression
- UART internal clocks enable/disable
- Auto baud rate detection (up to 115.2 Kbit/s)
- Receiver and transmitter enable/disable for power saving
- RX_DATA input and TX_DATA output can be inverted respectively in RS-232/RS-485 mode
- DCE/DTE capability
- RTS_B, IrDA asynchronous wake (AIRINT), receive asynchronous wake (AWAKE) interrupts wake the processor from STOP mode
- Maskable interrupts
- Two DMA Requests (TxFIFO DMA Request and RxFIFO DMA Request)
- Escape character sequence detection
- Software reset (SRST_B)
- Two independent, 32-entry FIFOs for transmit and receive
- The peripheral clock can be totally asynchronous with the module clock. The module clock determines baud rate. This allows frequency scaling on peripheral clock (such as during DVFS mode) while remaining the module clock frequency and baud rate.

Table 46: UART I/O Configuration vs. mode

Port	DTE Mode		DCE Mode	
	Direction	Description	Direction	Description
UARTx_RTS_B	Output	UARTx_RTS_B from DTE to DCE	Input	UARTx_RTS_B from DTE to DCE
UARTx_CTS_B	Input	UARTx_CTS_B from DCE to DTE	Output	UARTx_CTS_B from DCE to DTE
UARTx_TX_ DATA	Input	Serial data from DCE to DTE	Output	Serial data from DCE to DTE
UARTx_RX _DATA	Output	Serial data from DTE to DCE	Input	Serial data from DTE to DCE

8.10.1 UART1 Signals - SMARC SER0 pinout

Table 47: UART1 Signals - SMARC SER0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P129		SER0_TX	UART1_TXD(UART1_TX)	0		1.8V	SOC.AJ3
P130		SER0_RX	UART1_RXD(UART1_RX)	0		1.8V; PU 100K	SOC.AD6
P131		SER0_RTS#	UART3_RXD(UART1_CTS)	1		1.8V	SOC.AE6
P132		SER0_CTS#	UART3_TXD(UART1_RTS)	1		1.8V; PU 100K	SOC.AJ4

8.10.2 UART1 Signals – Proprietary SOM pinout (Non-SMARC)

Table 48: UART1 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P131		SER0_RTS#	UART3_RXD(UART1_CTS_B)	1		1.8V	SOC.AE6
S39		I2S0_LRCK	SAI2_TXFS(UART1_CTS_B)	4		1.8V	SOC.AJ17
S41		I2S0_SDIN	SAI2_RXD(UART1_RTS_B)	4		1.8V	SOC.AJ14
S142		GPIO12	SAI2_RXC(UART1_RX)	4	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(UART1_RX)	4	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
S123		GPIO13	SAI2_RXFS(UART1_TX)	4	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17
S151	CHG	CHARGING#	SAI2_RXFS(UART1_TX)	4	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17

8.10.3 UART2 Signals - SMARC SER1 pinout

Table 49: UART2 Signals - SMARC SER1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P134		SER1_TX	UART2_TXD(UART2_TX)	0	Used as debug UART on Variscite base board	1.8V	SOC.AH4
P135		SER1_RX	UART2_RXD(UART2_RX)	0	Used as debug UART on Variscite base board	1.8V; PU 100K	SOC.AF6

8.10.4 UART2 Signals – Proprietary SOM pinout (Non-SMARC)

Table 50: UART2 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P141		SER3_RX	UART4_RXD (UART2_CTS_B)	1		1.8V; PU 100K	SOC.AJ5
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(UART2_CTS_B)	4	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
P140		SER3_TX	UART4_TXD (UART2_RTS_B)	1		1.8V	SOC.AH5
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(UART2_RTS_B)	4	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
P39		SDIO_D0	SD2_DATA0(UART2_RX)	3		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(UART2_RX)	4	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
P40		SDIO_D1	SD2_DATA1(UART2_TX)	3		Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(UART2_TX)	4	Available in SOM without "AC" configuration;	1.8V	SOC.AH19

8.10.5 UART3 Signals - SMARC SER2 pinout

Table 51: UART3 Signals - SMARC SER2 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P136		SER2_TX	ECSPI1_MOSI(UART3_TX)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P137		SER2_RX	ECSPI1_SCLK(UART3_RX)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT	1.8V; PU 100K	SOC.AF20

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P138		SER2_RTS#	ECSPI1_MISO(UART3_CTS)	1	Function disabled Always exposed Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P139		SER2_CTS#	ECSPI1_SS0(UART3_RTS)	1	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20

8.10.6   UART3 Signals – Proprietary SOM pinout (Non-SMARC)

Table 52: UART3 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(UART3_RX)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P122		I2C_PM_DAT	SD1_DATA7(UART3_RX)	4		1.8V; PU 2.2K	SOC.U25
P131		SER0_RTS#	UART3_RXD(UART3_RX)	0		1.8V	SOC.AE6
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(UART3_TX)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P121		I2C_PM_CK	SD1_DATA6(UART3_TX)	4		1.8V; PU 2.2K	SOC.AA28
P132		SER0_CTS#	UART3_TXD(UART3_TX)	0		1.8V; PU 100K	SOC.AJ4

8.10.7   UART4 Signals – SMARC SER3 pinout

Table 53: UART4 Signals – SMARC SER3 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P140		SER3_TX	UART4_TXD(UART4_TX)	0		1.8V	SOC.AH5
P141		SER3_RX	UART4_RXD(UART4_RX)	0		1.8V; PU 100K	SOC.AJ5

8.10.8   UART4 Signals – Proprietary SOM pinout (Non-SMARC)

Table 54: UART4 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (UART4_CTS_B)	1	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
S56	QSPI	ESPI_IO_2 / QSPI_IO_2	NAND_DATA02(UART4_CTS_B)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.L24

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0 (UART4_RTS_B)	1	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
S57	QSPI	ESPI_IO_3 / QSPI_IO_3	NAND_DATA03(UART4_RTS_B)	3	Available in SOM with "QSPI" configuration;	1.8V	SOC.N24
P36		SDIO_CK	SD2_CLK(UART4_RX)	3		Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK (UART4_RX)	1	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(UART4_RX)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
P34		SDIO_CMD	SD2_CMD(UART4_TX)	3		Bank voltage set on SOM 1.8V/3.3V ; PU 10K	SOC.AB28
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(UART4_TX)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI (UART4_TX)	1	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21

8.11 Flexible Controller Area Network

The Flexible Controller Area Network (FLEXCAN) module is a communication controller supporting CAN-FD (CAN Flexible Data Rate) and CAN2.0B specification.

Note: CAN-FD is supported only on Industrial variant of the SOM, Consumer variant of the SOM supports only CAN.

Signal Description:

- CAN Rx: The receive pin from the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.
- CAN Tx: The transmit pin to the CAN bus transceiver. Dominant state is represented by logic level '0'. Recessive state is represented by logic level '1'.

The SMARC specification defines 2x CAN interfaces CAN0, CAN1 these are mapped to the i.MX8M-PLUS SoC FLEXCAN1, FLEXCAN2 interfaces respectively.

8.11.1 FLEXCAN1 Signals – SMARC CAN0 pinout

Table 55: FLEXCAN1 Signals - SMARC CAN0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P143		CAN0_TX	SPDIF_TX(FLEXCAN1_TX)	4		1.8V	SOC.AE18
P144		CAN0_RX	SPDIF_RX(FLEXCAN1_RX)	4		1.8V	SOC.AD18

8.11.2 FLEXCAN1 Signals – Proprietary SOM pinout (Non-SMARC)

Table 56: FLEXCAN1 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P106		HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA(FLEXCAN1_RX)	4		1.8V	SOC.AF22
S42		I2S0_CK	SAI2_TXC(FLEXCAN1_RX)	3		1.8V	SOC.AH15
P105		HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL(FLEXCAN1_TX)	4		1.8V	SOC.AC22
S142		GPIO12	SAI2_RXC(FLEXCAN1_TX)	3	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(FLEXCAN1_TX)	3	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16

8.11.3 FLEXCAN2 Signals – SMARC CAN1 pinout

Table 57: FLEXCAN2 Signals - SMARC CAN1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P145		CAN1_TX	HDMI_CEC(FLEXCAN2_TX)	4		1.8V	SOC.AD22
P146		CAN1_RX	SAI5_MCLK(CAN2_RX)	6		1.8V	SOC.AF14

8.11.4 FLEXCAN2 Signals – Proprietary SOM pinout (Non-SMARC)

Table 58: FLEXCAN2 Signals -Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P104		HDMI_HPD / DP1_HPD	HDMI_HPD (FLEXCAN2_RX)	4		1.8V	SOC.AE22
P132		SER0_CTS#	UART3_TXD(FLEXCAN2_RX)	4		1.8V; PU 100K	SOC.AJ4
S38		AUDIO_MCK	SAI2_MCLK(FLEXCAN2_RX)	3		1.8V	SOC.AJ15
P131		SER0_RTS#	UART3_RXD(FLEXCAN2_TX)	4		1.8V	SOC.AE6
S40		I2S0_SDOUT	SAI2_TXD(FLEXCAN2_TX)	3		1.8V	SOC.AH16

8.12 ECSPI - Enhanced Configurable SPI

The VAR-SMARC-MX8M-PLUS exposes all 3x ECSPI interfaces.

The Enhanced Configurable Serial Peripheral Interface (ECSPI) is a full-duplex, synchronous, four-wire serial communication block with full-duplex enhanced Synchronous Serial Interface and data rate up to 52 Mbit/s.

Key features of the ECSPI include:
- Full-duplex synchronous serial interface
- Master/Slave configurable
- One native Chip Select (SS) signal [see note below]
- Transfer continuation function allows unlimited length data transfers
- 32-bit wide by 64-entry FIFO for both transmit and receive data
- Polarity and phase of the Chip Select (SS) and SPI Clock (SCLK) are configurable
- Direct Memory Access (DMA) support
- Refer to the product data sheet for the maximum operating frequency

Note: Note: For interacting with multiple peripherals on same SPI bus, one can define any GPIO to be used as chip select. Examples can be found in our DTS files.

The SMARC specification defines 2x SPI interfaces SPI0, SPI1 these are mapped to the i.MX8M-PLUS ECSPI1, ECSPI2 respectively.

8.12.1 ESCPI1 Signals - SMARC SPI0 pinout

Note: ECSPI1 interface is used by WIFI module in **"WBE"** configurations
ECSPI1 interface can be used externally only if 802.15.4 (LR-WPAN) interface is disabled of SOMs with **"no WBE"**. For further information refer to section "8.5 Wi-Fi & BT".

Table 59: ECSPI1 Signals -SMARC SPI0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P31		SPI0_CS1#	SAI1_MCLK(GPIO4_IO20)	5		1.8V	SOC.AE12
P43	no WBE	SPI0_CS0#	I2C2_SDA(ECSPI1_SS0)	3	Available in SOM without "WBE" configuration; Available in SOM with "WBE" configuration;	1.8V	SOC.AE8
P43	WBE	SPI0_CS0#	GPIO1_IO00	0	Duplicate pin on P115;	1.8V	SOC.A7
P44		SPI0_CK	I2C1_SCL(ECSPI1_SCLK0)	0		1.8V	SOC.AC8
P45		SPI0_DIN	I2C2_SCL(ECSPI1_MISO)	3		1.8V	SOC.AH6
P46		SPI0_DO	I2C1_SDA(ECSPI1_MOSI)	3		1.8V	SOC.AH7

8.12.2 ESCPI1 Signals – Proprietary SOM pinout (Non-SMARC)

Table 60: ECSPI1 Signals– Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P138		SER2_RTS#	ECSPI1_MISO(ECSPI1_MISO)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P136		SER2_TX	ECSPI1_MOSI(ECSPI1_MOSI)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P137		SER2_RX	ECSPI1_SCLK(ECSPI1_SCLK)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AF20
P139		SER2_CTS#	ECSPI1_SS0(ECSPI1_SS0)	0	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20

8.12.3 ESCPI2 Signals – SMARC SPI1 pinout

Table 61: ECSPI2 Signals – SMARC SPI1 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0	0	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(GPIO3_IO14)_QSPI_A_DQS	5		1.8V	SOC.R26
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK	0	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO	0	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI	0	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21

8.12.4 ESCPI2 Signals – Proprietary SOM pinout (Non-SMARC)

Table 62: ECSPI2 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P42		SDIO_D3	SD2_DATA3(ECSPI2_MISO)	2		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
S48		I2C_GP_CK	I2C4_SCL (ECSPI2_MISO)	3	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
P34		SDIO_CMD	SD2_CMD(ECSPI2_MOSI)	2		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AB28
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(ECSPI2_MOSI)	3		1.8V; PU 2.2K	SOC.AJ6
P36		SDIO_CK	SD2_CLK(ECSPI2_SCLK)	2		Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(ECSPI2_SCLK)	3		1.8V; PU 2.2K	SOC.AJ7
P41		SDIO_D2	SD2_DATA2(ECSPI2_SS0)	2		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
S49		I2C_GP_DAT	I2C4_SDA (ECSPI2_SS0)	3	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8

8.12.5 ESCPI3 Signals – Proprietary SOM pinout (Non-SMARC)

Table 63: ECSPI3 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P135		SER1_RX	UART2_RXD (ECSPI3_MISO)	1	Used as debug UART on Variscite base board	1.8V; PU 100K	SOC.AF6
P129		SER0_TX	UART1_TXD (ECSPI3_MOSI)	1		1.8V	SOC.AJ3
P130		SER0_RX	UART1_RXD (ECSPI3_SCLK)	1		1.8V; PU 100K	SOC.AD6
P134		SER1_TX	UART2_TXD (ECSPI3_SS0)	1	Used as debug UART on Variscite base board	1.8V	SOC.AH4

8.13 QSPI/FlexSPI - Quad Serial Peripheral Interface

The VAR-SMARC-MX8M-PLUS exposes one QSPI module which can be used to interface external serial flash devices.

The module contains the following features:

- Flexible sequence engine to support various flash vendor devices
- Single pad/Dual pad/Quad pad mode of operation
- Single Data Rate/Double Data Rate mode of operation
- Parallel Flash mode
- DMA support
- Memory mapped read access to connected flash devices
- Multi master access with priority and flexible and configurable buffer for each master

Note: QSPI signals are available on SOM with "QSPI" assembly option.

The SMARC specification defines 1x QSPI interface which is mapped to the i.MX8M-PLUS QSPIA interface.

8.13.1 QSPIA Signals – SMARC QSPI pinout

Table 64: QSPIA Signals – SMARC QSPI pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(QSPI_A_SS0_B)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(GPIO3_IO14)_QSPI_A_DQS	5		1.8V	SOC.R26
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(QSPI_A_SCLK)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(QSPI_A_DATA1)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(QSPI_A_DATA0)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
S56	QSPI	ESPI_IO_2 / QSPI_IO_2	NAND_DATA02(QSPI_A_DATA2)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.L24
S57	QSPI	ESPI_IO_3 / QSPI_IO_3	NAND_DATA03(QSPI_A_DATA3)	1	Available in SOM with "QSPI" configuration;	1.8V	SOC.N24

8.14 PWM

The VAR-SMARC-MX8M-PLUS exports up to 4 General purpose Pulse Width Modulators (PWM) signals.

PWM Features:

- 16-bit up-counter with clock source selection (bus clock, baud clock, or 32K)
- 4 x 16 FIFO to minimize interrupt overhead
- 12-bit prescaler for division of clock
- Sound and melody generation
- Active high or active low configured output
- Can be programmed to be active in low-power mode
- Can be programmed to be active in debug mode
- Interrupts at compare and rollover

The SMARC specification defines 3x PWM interface PWM_OUT/ LCD0_BKLT_PWM/ LCD1_BKLT_PWM these are mapped to the i.MX8M-PLUS PWM3/2/1 interfaces respectively.

8.14.1 PWM Signals – SMARC PWM_OUT/ LCDx_BKLT_PWM pinout

Table 65: PWM Signals - SMARC PWM_OUT/ LCDx_BKLT_PWM pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P113		GPIO5 / PWM_OUT	GPIO1_IO14(PWM3_OUT)	5		1.8V	SOC.A4
S122		LCD1_BKLT_PWM	GPIO1_IO11(PWM2_OUT)	2		1.8V	SOC.D8
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(PWM1_OUT)	1		1.8V	SOC.AC18

8.14.2 PWM Signals – Proprietary SOM pinout (Non-SMARC)

Table 66: PWM Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P37		SDIO_PWR_EN	GPIO1_IO08_3V3 (PWM1_OUT)	2	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P117		GPIO9	GPIO1_IO01 (PWM1_OUT)	1		1.8V	SOC.E8
P146		CAN1_RX	SAI5_MCLK(PWM1_OUT)	2		1.8V	SOC.AF14
S49		I2C_GP_DAT	I2C4_SDA (PWM1_OUT)	1	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8
P6		GBE0_SDP	GPIO1_IO09(PWM2_OUT)_3V3	2	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)
P62		USB0_EN_OC#	GPIO1_IO13_3V3 (PWM2_OUT)	5	SoC USB1 - USB0 Over-Current Sense GPIO;	3.3V, via bidirectional OD level	SOC.A6 (via bidirectional OD

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
						shifter; with 10K PU	level shifter)
P144		CAN0_RX	SPDIF_RX(PWM2_OUT)	1		1.8V	SOC.AD18
S48		I2C_GP_CK	I2C4_SCL (PWM2_OUT)	1	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
P64		USB0_OTG_ID	GPIO1_IO10(PWM3_OUT)_3V3	2	SoC USB1 - USB0_OTG_ID GPIO;	3.3V, Input via push pull level shifter	SOC.B7 (via push pull level shifter)
P143		CAN0_TX	SPDIF_TX(PWM3_OUT)	1		1.8V	SOC.AE18
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(PWM3_OUT)	2	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(PWM3_OUT)	1		1.8V; PU 2.2K	SOC.AJ6
S140		I2C_LCD_DAT	SAI5_RXC(PWM3_OUT)	2	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(PWM4_OUT)	2	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(PWM4_OUT)	1		1.8V; PU 2.2K	SOC.AJ7
S6		CAM_MCK	GPIO1_IO15(PWM4_OUT)	5		1.8V	SOC.B5
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (PWM4_OUT)	1	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
S139		I2C_LCD_CK	SAI5_RXFS(PWM4_OUT)	2	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14

8.15 I2C

The VAR-SMARC-MX8M-PLUS exposes up to 5x I2C Interface connectivity peripherals which provides serial interface for external devices. Data rates of up to 400 kbps are supported.

The Inter-Integrated Circuit (I2C) provides functionality of a standard I2C master and slave. I2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices.
This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I2C standard allows additional devices to be connected to the bus for expansion and system development.

The I2C has the following key features:
- Compatible with the I2C Bus Specification, version 2.1, by Philips Semiconductor (now NXP Semiconductors).
- Multi-master operation.
- After a reset, the I2C defaults to Slave Receive operations.
- Software programmability for one of 64 different serial clock frequencies:
    o Standard mode, I2C supports the data transfer rates up to 100 Kbits/s
    o In Fast mode, data transfer rates up to 400 Kbits/s can be achieved
- Software-selectable acknowledge bit
- Interrupt-driven, byte-by-byte data transfer
- Arbitration-lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated start signal generation
- Acknowledge bit generation/detection
- Bus-busy detection

The SMARC specification defines up to 8x I2C interfaces.

5x SMARC I2C interfaces: I2C_PM/ I2C_CAM0/I2C_CAM1/ I2C_GP/ I2C_LCD are mapped to the i.MX8M-PLUS SoC I2C2/6/3/4/6 interfaces respectively.

8.15.1 I2C1 Signals

I2C1 is used internally by on-SOM EEPROM used for boot process and by Audio codec.
Using it externally from SOM pins which have the I2C1 alternate function in not allowed.

8.15.2 I2C2 Signals – SMARC I2C_PM pinout

Table 67: I2C2 Signals – SMARC I2C_PM pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P121		I2C_PM_CK	SD1_DATA6(I2C2_SCL)	3		1.8V; PU 2.2K	SOC.AA28
P122		I2C_PM_DAT	SD1_DATA7(I2C2_SDA)	3		1.8V; PU 2.2K	SOC.U25

8.15.3 I2C2 Signals - Proprietary SOM pinout (Non-SMARC)

Table 68: I2C2 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P45		SPI0_DIN	I2C2_SCL(I2C2_SCL)	0		1.8V	SOC.AH6
P138		SER2_RTS#	ECSPI1_MISO(I2C2_SCL)	2	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P43	no WBE	SPI0_CS0#	I2C2_SDA(I2C2_SDA)	0	Available in SOM without "WBE" configuration;	1.8V	SOC.AE8
P139		SER2_CTS#	ECSPI1_SS0(I2C2_SDA)	2	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20

8.15.4 I2C3 Signals – SMARC I2C_CAM0 pinout

Table 69: I2C3 Signals – SMARC I2C_CAM0 pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(I2C3_SCL)	0		1.8V; PU 2.2K	SOC.AJ7
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(I2C3_SDA)	0		1.8V; PU 2.2K	SOC.AJ6

8.15.5 I2C3 Signals - Proprietary SOM pinout (Non-SMARC)

Table 70: I2C3 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(I2C3_SCL)_QSPI_A_DQS	4		1.8V	SOC.R26
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK (I2C3_SCL)	2	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI (I2C3_SDA)	2	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21

8.15.6 I2C4 Signals – SMARC I2C_GP pinout

Table 71: I2C4 Signals – SMARC I2C_GP pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S48		I2C_GP_CK	I2C4_SCL	0	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
S49		I2C_GP_DAT	I2C4_SDA	0	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8

8.15.7 I2C4 Signals – Proprietary SOM pinout (Non-SMARC)

Table 72: I2C4 Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P40		SDIO_D1	SD2_DATA1(I2C4_SCL)	2		Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (I2C4_SCL)	2	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
S48		I2C_GP_CK	I2C4_SCL (I2C4_SCL)	0	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
P39		SDIO_D0	SD2_DATA0(I2C4_SDA)	2		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0 (I2C4_SDA)	2	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
S49		I2C_GP_DAT	I2C4_SDA (I2C4_SDA)	0	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8
S56	QSPI	ESPI_IO_2 / QSPI_IO_2	NAND_DATA02(I2C4_SDA)	4	Available in SOM with "QSPI" configuration;	1.8V	SOC.L24

8.15.8 I2C5 Signals - Proprietary SOM pinout (Non-SMARC)

Table 73: I2C5 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P105		HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL(I2C5_SCL)	3		1.8V	SOC.AC22
P143		CAN0_TX	SPDIF_TX(I2C5_SCL)	2		1.8V	SOC.AE18
P106		HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA(I2C5_SDA)	3		1.8V	SOC.AF22
P144		CAN0_RX	SPDIF_RX(I2C5_SDA)	2		1.8V	SOC.AD18
P146		CAN1_RX	SAI5_MCLK(I2C5_SDA)	3		1.8V	SOC.AF14

8.15.9 I2C6 Signals - SMARC I2C_CAM1/I2C_LCD pinout

Table 74: I2C6 Signals - SMARC I2C_CAM1/I2C_LCD pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(I2C6_SCL)	3	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S139		I2C_LCD_CK	SAI5_RXFS(I2C6_SCL)	3	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(I2C6_SDA)	3	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S140		I2C_LCD_DAT	SAI5_RXC(I2C6_SDA)	3	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14

8.15.10 I2C6 Signals - Proprietary SOM pinout (Non-SMARC)

Table 75: I2C6 Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P141		SER3_RX	UART4_RXD (I2C6_SCL)	4		1.8V; PU 100K	SOC.AJ5
P145		CAN1_TX	HDMI_CEC(I2C6_SCL)	3		1.8V	SOC.AD22
P104		HDMI_HPD / DP1_HPD	HDMI_HPD (I2C6_SDA)	3		1.8V	SOC.AE22
P140		SER3_TX	UART4_TXD (I2C6_SDA)	4		1.8V	SOC.AH5

8.16 General Purpose Timer

The VAR-SMARC-MX8M-PLUS exposes the GPT interface to its connector.

GPT Features include:
- One 32-bit up-counter with clock source selection, including external clock
- Two input capture channels with a programmable trigger edge
- Three outputs compare channels with a programmable output mode. A "forced compare" feature is also available
- Can be programmed to be active in low power and debug modes
- Interrupt generation at capture, compare, and rollover events
- Restart or free-run modes for counter operations

8.16.1.1 GPT Signals – Proprietary SOM pinout (Non-SMARC)

Table 76: GPT Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P140		SER3_TX	UART4_TXD (GPT1_CAPTURE1)	3		1.8V	SOC.AH5
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(GPT1_CAPTURE1)	3	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
P131		SER0_RTS#	UART3_RXD(GPT1_CAPTURE2)	3		1.8V	SOC.AE6
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(GPT1_CAPTURE2)	3	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
P132		SER0_CTS#	UART3_TXD(GPT1_CLK)	3		1.8V; PU 100K	SOC.AJ4
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(GPT1_CLK)	3	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
P141		SER3_RX	UART4_RXD (GPT1_COMPARE1)	3		1.8V; PU 100K	SOC.AJ5
P143		CAN0_TX	SPDIF_TX(GPT1_COMPARE1)	3		1.8V	SOC.AE18
P134		SER1_TX	UART2_TXD (GPT1_COMPARE2)	3	Used as debug UART on Variscite base board	1.8V	SOC.AH4
P144		CAN0_RX	SPDIF_RX(GPT1_COMPARE2)	3		1.8V	SOC.AD18
P135		SER1_RX	UART2_RXD (GPT1_COMPARE3)	3	Used as debug UART on Variscite base board	1.8V; PU 100K	SOC.AF6
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(GPT1_COMPARE3)	3		1.8V	SOC.AC18
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(GPT2_CLK)	2		1.8V; PU 2.2K	SOC.AJ7
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(GPT3_CLK)	2		1.8V; PU 2.2K	SOC.AJ6

8.17 Reference Clocks

The VAR-SMARC-MX8M-PLUS exposes the clock outputs from the internal CCM module which can be used to clock external devices.

8.17.1 Clock Signals – Proprietary SOM pinout (Non-SMARC)

Table 77: Clock Signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (CCM_CLKO1)	4	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
P113		GPIO5 / PWM_OUT	GPIO1_IO14(CCM_CLKO1)	6		1.8V	SOC.A4
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0 (CCM_CLKO2)	4	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
S6		CAM_MCK	GPIO1_IO15(CCM_CLKO2)	6		1.8V	SOC.B5
P43	WBE	SPI0_CS0#	GPIO1_IO00 (CCM_ENET_PHY_REF_CLK_ROOT)	1	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
P115		GPIO7	GPIO1_IO00 (CCM_ENET_PHY_REF_CLK_ROOT)	1	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
P43	WBE	SPI0_CS0#	GPIO1_IO00 (CCM_EXT_CLK1)	6	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
P115		GPIO7	GPIO1_IO00 (CCM_EXT_CLK1)	6	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
P117		GPIO9	GPIO1_IO01 (CCM_EXT_CLK2)	6		1.8V	SOC.E8
P119		GPIO11	GPIO1_IO06 (CCM_EXT_CLK3)	6	In SOM with "CHG" configuration, Duplicate pin on S156;	1.8V	SOC.A3
S156	CHG	BATLOW#	GPIO1_IO06 (CCM_EXT_CLK3)	6	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
P118		GPIO10	GPIO1_IO07 (CCM_EXT_CLK4)	6		1.8V	SOC.F6
P114		GPIO6 / TACHIN	GPIO1_IO05 (CCM_PMIC_READY)	5		1.8V	SOC.B4
S122		LCD1_BKLT_PWM	GPIO1_IO11(CCM_PMIC_READY)	5		1.8V	SOC.D8
P117		GPIO9	GPIO1_IO01 (CCM_REF_CLK_24M)	5		1.8V	SOC.E8
P43	WBE	SPI0_CS0#	GPIO1_IO00 (CCM_REF_CLK_32K)	5	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
P115		GPIO7	GPIO1_IO00 (CCM_REF_CLK_32K)	5	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2 (ENET_QOS_INPUT=ENET_QOS_TX_CLK OUTPUT=CCM_ENET_QOS_REF_CLK_ROOT)	1	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P31		SPI0_CS1#	SAI1_MCLK(ENET1_INPUT=ENET1_TX_CLK OUTPUT=CCM_ENET_REF_CLK_ROOT)	4		1.8V	SOC.AE12

8.18   JTAG

The VAR-SMARC-MX8M-PLUS consists of the System JTAG Controller (SJC) which provides debug and test control with maximum security. The test access port (TAP) is designed to support features compatible with the IEEE standard 1149.1 v2001 (JTAG) and IEEE 1149.6 standards.

The JTAG port allows debug-related control and status, such as putting selected cores into reset and/or debug mode and the ability to monitor individual core status signals via JTAG.
JTAG port interfaces the M7 and Cortex A53 Cores DAP - debug access port.
The VAR-SMARC-MX8M-PLUS JTAG_MOD pin is hardware tied low and enables the Daisy chain ALL mode only, used for common SW debug (High speed and production).

VAR-SMARC-MX8M-PLUS exposes JTAG signals on -pin connector (not assembled by default) JST P/N: SM10B-SRSS-TB) located on the SOM top left side.

The SMARC specification defines the 1x JTAG interface which is mapped to the i.MX8M-PLUS SoC JTAG interface.

8.18.1   JTAG Signals – SMARC JTAG pinout

Figure 6 : JTAG signals on 10-pin Header Connector
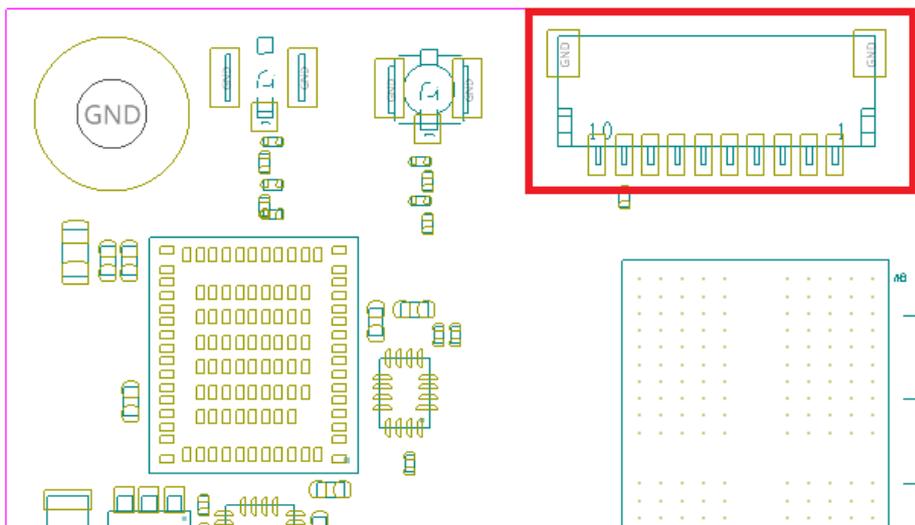
Table 78: JTAG signals - SMARC JTAG pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
1	JTAG	VDD_JTAG	VTREF		Available in SOM with "JTAG" configuration; JTAG reference voltage (1.8v)	1.8V via 100R Res.	VTREF
2	JTAG	JTAG_TRST#	NC		Available in SOM with "JTAG" configuration;		NC
3	JTAG	JTAG_TMS	JTAG_TMS	0	Available in SOM with "JTAG" configuration; JTAG Test Mode select	1.8V; PU 10K	SOC.G14
4	JTAG	JTAG_TDO	JTAG_TDO	0	Available in SOM with "JTAG" configuration; JTAG Test Data Out	1.8V	SOC.F14
5	JTAG	JTAG_TDI	JTAG_TDI	0	Available in SOM with "JTAG" configuration; JTAG Test Data In	1.8V; PU 10K	SOC.G16
6	JTAG	JTAG_TCK	JTAG_TCK	0	Available in SOM with "JTAG" configuration; JTAG Test Clock	1.8V	SOC.G18
7	JTAG	TAG_RTCK	NC		Available in SOM with "JTAG" configuration;		NC
8	JTAG	JTAG_RESET_IN#	PMIC_RST_B	0	Available in SOM with "JTAG" configuration; SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset.	1.8V, Input via diode; PU 10K	PCA9450C HNY.8 via diode; J1.8
9	JTAG	MFG_MODE#	NC		Available in SOM with "JTAG" configuration;		NC
10	JTAG	GND	GND		Available in SOM with "JTAG" configuration; Digital Ground		GND

8.19 General Purpose IO

The SMARC specification defines 14 GPIOs: GPIO0-GIO13 which are provided by the VAR-SMARC-MX8M-PLUS.
Additional GPIOs, if required, can be exported from other SOM pins.

8.19.1 GPIO Signals – SMARC GPIO[0:13] pinout

Table 79: GPIO Signals - SMARC GPIO[0:13] pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P108		GPIO0 / CAM0_PWR#	GPIO_EXP_P0_0__GPIO0_CAM0_PWR#	0	Signal source is GPIO Expander P0_0;	1.8V	PCAL6416 AHF,128.1
P109		GPIO1 / CAM1_PWR#	GPIO_EXP_P0_1__GPIO1_CAM1_PWR#	0	Signal source is GPIO Expander P0_1;	1.8V	PCAL6416 AHF,128.2
P110		GPIO2 / CAM0_RST#	GPIO_EXP_P0_2__GPIO2_CAM0_RST#	0	Signal source is GPIO Expander P0_2;	1.8V	PCAL6416 AHF,128.3
P111		GPIO3 / CAM1_RST#	GPIO_EXP_P0_3__GPIO3_CAM1_RST#	0	Signal source is GPIO Expander P0_3;	1.8V	PCAL6416 AHF,128.4
P112		GPIO4 / HDA_RST#	GPIO1_IO03	0		1.8V	SOC.D6
P113		GPIO5 / PWM_OUT	GPIO1_IO14(PWM3_OUT)	5		1.8V	SOC.A4
P114		GPIO6 / TACHIN	GPIO1_IO05	0		1.8V	SOC.B4
P115		GPIO7	GPIO1_IO00	0	in SOM with "WBE" configuration, Duplicate pin on P43;	1.8V	SOC.A7
P116		GPIO8	SAI1_RXD0(GPIO4_IO02)	5		1.8V	SOC.AC10
P117		GPIO9	GPIO1_IO01	0		1.8V	SOC.E8
P118		GPIO10	GPIO1_IO07	0		1.8V	SOC.F6
P119		GPIO11	GPIO1_IO06	0	In SOM with "CHG" configuration, Duplicate pin on S156;	1.8V	SOC.A3
S142		GPIO12	SAI2_RXC(GPIO4_IO22)	5	In SOM with "CHG" configuration, Duplicate pin on S152;	1.8V	SOC.AJ16
S123		GPIO13	SAI2_RXFS(GPIO4_IO21)	5	In SOM with "CHG" configuration, Duplicate pin on S151;	1.8V	SOC.AH17

8.19.2   GPIO Signals – Proprietary SOM pinout (Non-SMARC)

Table 80: GPIO Signals - Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P43	WBE	SPI0_CS0#	GPIO1_IO00 (GPIO1_IO00)	0	Available in SOM with "WBE" configuration; Duplicate pin on P115;	1.8V	SOC.A7
S145		WDT_TIME_OUT#	WDOG_B (GPIO1_IO02)	0		1.8V	SOC.B6
S156	CHG	BATLOW#	GPIO1_IO06 (GPIO1_IO06)	0	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
P37		SDIO_PWR_EN	GPIO1_IO08_3V3 (GPIO1_IO08)	0	SDIO PWR enable GPIO;	3.3V, Output via push pull level shifter; with 10K PU	SOC.A8 (via push pull level shifter)
P6		GBE0_SDP	GPIO1_IO09(GPIO1_IO09)_3V3	0	GBE0 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.B8 (via push pull level shifter)
P64		USB0_OTG_ID	GPIO1_IO10(GPIO1_IO10)_3V3	0	SoC USB1 - USB0_OTG_ID GPIO;	3.3V, Input via push pull level shifter	SOC.B7 (via push pull level shifter)
S122		LCD1_BKLT_PWM	GPIO1_IO11(GPIO1_IO11)	0		1.8V	SOC.D8
P62		USB0_EN_OC#	GPIO1_IO13_3V3 (GPIO1_IO13)	0	SoC USB1 - USB0 Over-Current Sense GPIO;	3.3V, via bidirectional OD level shifter; with 10K PU	SOC.A6 (via bidirectional OD level shifter)
S6		CAM_MCK	GPIO1_IO15(GPIO1_IO15)	0		1.8V	SOC.B5
S45		MDIO_CLK	ENET_QOS_MDC (GPIO1_IO16)	5	GBE1/2 MDIO Clock Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V	SOC.AH28
S46		MDIO_DAT	ENET_QOS_MDIO (GPIO1_IO17)	5	GBE1/2 MDIO Data Signal; Pin alternate function cannot be changed when using SOM with EC assembled Do not alter pinmux with "EC1" or "EC2" configuration	1.8V; PU 1.47K	SOC.AH29
P30	no EC1	GBE0_MDI0+	ENET_QOS_RGMII_TD3 (GPIO1_IO18)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AD24
P29	no EC1	GBE0_MDI0-	ENET_QOS_RGMII_TD2 (GPIO1_IO19)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AF26
P27	no EC1	GBE0_MDI1+	ENET_QOS_RGMII_TD1 (GPIO1_IO20)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AE26
P26	no EC1	GBE0_MDI1-	ENET_QOS_RGMII_TD0 (GPIO1_IO21)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AC25
S54	no EC1	SATA_ACT#	ENET_QOS_RGMII_TX_CTL (GPIO1_IO22)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AH13

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P21	no EC1	GBE0_LINK_MID#	ENET_QOS_RGMII_TXC (GPIO1_IO23)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AE24
P25	no EC1	GBE0_LINK_ACT#	ENET_QOS_RGMII_RX_CTL (GPIO1_IO24)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AE28
P22	no EC1	GBE0_LINK_MAX#	ENET_QOS_RGMII_RXC (GPIO1_IO25)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AE29
P24	no EC1	GBE0_MDI2+	ENET_QOS_RGMII_RD0 (GPIO1_IO26)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AG29
P23	no EC1	GBE0_MDI2-	ENET_QOS_RGMII_RD1 (GPIO1_IO27)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AG28
P20	no EC1	GBE0_MDI3+	ENET_QOS_RGMII_RD2 (GPIO1_IO28)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AF29
P19	no EC1	GBE0_MDI3-	ENET_QOS_RGMII_RD3 (GPIO1_IO29)	5	Available in SOM without "EC1" configuration;	1.8V	SOC.AF28
P121		I2C_PM_CK	SD1_DATA6(GPIO2_IO08)	5		1.8V; PU 2.2K	SOC.AA28
P122		I2C_PM_DAT	SD1_DATA7(GPIO2_IO09)	5		1.8V; PU 2.2K	SOC.U25
P35		SDIO_CD#	SD2_CD_B(GPIO2_IO12)	5		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AD29
P36		SDIO_CK	SD2_CLK(GPIO2_IO13)	5		Bank voltage set on SOM 1.8V/3.3V	SOC.AB29
P34		SDIO_CMD	SD2_CMD(GPIO2_IO14)	5		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AB28
P39		SDIO_D0	SD2_DATA0(GPIO2_IO15)	5		Bank voltage set on SOM 1.8V/3.3V	SOC.AC28
P40		SDIO_D1	SD2_DATA1(GPIO2_IO16)	5		Bank voltage set on SOM 1.8V/3.3V	SOC.AC29
P41		SDIO_D2	SD2_DATA2(GPIO2_IO17)	5		Bank voltage set on SOM 1.8V/3.3V	SOC.AA26
P42		SDIO_D3	SD2_DATA3(GPIO2_IO18)	5		Bank voltage set on SOM 1.8V/3.3V	SOC.AA25
P33		SDIO_WP	SD2_WP(GPIO2_IO20)	5		Bank voltage set on SOM 1.8V/3.3V; PU 10K	SOC.AC26

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P56	QSPI	SPI1_CK / ESPI_CK / QSPI_CK	NAND_ALE(GPIO3_IO00)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.N25
P54	QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	NAND_CE0_B(GPIO3_IO01)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.L26
P58	QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	NAND_DATA00(GPIO3_IO06)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.R25
P57	QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	NAND_DATA01(GPIO3_IO07)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.L25
S56	QSPI	ESPI_IO_2 / QSPI_IO_2	NAND_DATA02(GPIO3_IO08)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.L24
S57	QSPI	ESPI_IO_3 / QSPI_IO_3	NAND_DATA03(GPIO3_IO09)	5	Available in SOM with "QSPI" configuration;	1.8V	SOC.N24
P55		SPI1_CS1# / ESPI_CS1# / QSPI_CS1#	NAND_DQS(GPIO3_IO14)_QSPI_A_DQS	5		1.8V	SOC.R26
S1		CSI1_TX+ / I2C_CAM1_CK	SAI5_RXFS(GPIO3_IO19)	5	Duplicate pin on S139;	1.8V; PU 2.2K	SOC.AC14
S139		I2C_LCD_CK	SAI5_RXFS(GPIO3_IO19)	5	Duplicate pin on S1;	1.8V; PU 2.2K	SOC.AC14
S2		CSI1_TX- / I2C_CAM1_DAT	SAI5_RXC(GPIO3_IO20)	5	Duplicate pin on S140;	1.8V; PU 2.2K	SOC.AD14
S140		I2C_LCD_DAT	SAI5_RXC(GPIO3_IO20)	5	Duplicate pin on S2;	1.8V; PU 2.2K	SOC.AD14
P146		CAN1_RX	SAI5_MCLK(GPIO3_IO25)	5		1.8V	SOC.AF14
P105		HDMI_CTRL_CK / DP1_AUX+	HDMI_DDC_SCL(GPIO3_IO26)	5		1.8V	SOC.AC22
P106		HDMI_CTRL_DAT / DP1_AUX-	HDMI_DDC_SDA(GPIO3_IO27)	5		1.8V	SOC.AF22
P145		CAN1_TX	HDMI_CEC(GPIO3_IO28)	5		1.8V	SOC.AD22
P104		HDMI_HPD / DP1_HPD	HDMI_HPD (GPIO3_IO29)	5		1.8V	SOC.AE22
S149		SLEEP#	SAI1_RXFS(GPIO4_IO00)	5		1.8V; PU 10K	SOC.AJ9
P5		GBE1_SDP	SAI1_RXC(GPIO4_IO01)_3V3	5	GBE1 IEEE 1588 Trigger Signal;	3.3V, Output via push pull level shifter	SOC.AH8 (via push pull level shifter)
S148		LID#	SAI1_TXD6(GPIO4_IO18)	5		1.8V; PU 10K	SOC.AC12
P1		SMB_ALERT#	SAI1_TXD7(GPIO4_IO19)	5		1.8V; PU 2.2K	SOC.AJ13
P31		SPI0_CS1#	SAI1_MCLK(GPIO4_IO20)	5		1.8V	SOC.AE12
S151	CHG	CHARGING#	SAI2_RXFS(GPIO4_IO21)	5	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(GPIO4_IO22)	5	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
S41		I2S0_SDIN	SAI2_RXD(GPIO4_IO23)	5		1.8V	SOC.AJ14
S39		I2S0_LRCK	SAI2_TXFS(GPIO4_IO24)	5		1.8V	SOC.AJ17
S42		I2S0_CK	SAI2_TXC(GPIO4_IO25)	5		1.8V	SOC.AH15
S40		I2S0_SDOUT	SAI2_TXD(GPIO4_IO26)	5		1.8V	SOC.AH16
S38		AUDIO_MCK	SAI2_MCLK(GPIO4_IO27)	5		1.8V	SOC.AJ15

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S43	no AC & SAI3	ESPI_ALERT0#	SAI3_RXFS(GPIO4_IO28)	5	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ19
S44	no AC & SAI3	ESPI_ALERT1#	SAI3_RXC(GPIO4_IO29)	5	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ18
S52	no AC	I2S2_SDIN / HDA_SDI / SNDW_DAT0	SAI3_RXD(GPIO4_IO30)	5	Available in SOM without "AC" configuration;	1.8V	SOC.AF18
S50	no AC	I2S2_LRCK / HDA_SYNC / SNDW_CLK1	SAI3_TXFS(GPIO4_IO31)	5	Available in SOM without "AC" configuration;	1.8V	SOC.AC16
S53	no AC	I2S2_CK / HDA_CK / SNDW_CLK0	SAI3_TXC(GPIO5_IO00)	5	Available in SOM without "AC" configuration;	1.8V	SOC.AH19
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(GPIO5_IO01)	5	Available in SOM without "AC" configuration;	1.8V	SOC.AH18
S58	no AC & SAI3	ESPI_RESET#	SAI3_MCLK (GPIO5_IO02)	5	Available in SOM without "AC" and with "SAI3" configuration;	1.8V	SOC.AJ20
P143		CAN0_TX	SPDIF_TX(GPIO5_IO03)	5		1.8V	SOC.AE18
P144		CAN0_RX	SPDIF_RX(GPIO5_IO04)	5		1.8V	SOC.AD18
S141		LCD0_BKLT_PWM	SPDIF_EXT_CLK(GPIO5_IO05)	5		1.8V	SOC.AC18
P137		SER2_RX	ECSPI1_SCLK(GPIO5_IO06)	5	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AF20
P136		SER2_TX	ECSPI1_MOSI(GPIO5_IO07)	5	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AC20
P138		SER2_RTS#	ECSPI1_MISO(GPIO5_IO08)	5	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V	SOC.AD20
P139		SER2_CTS#	ECSPI1_SS0(GPIO5_IO09)	5	Used internally with "WBD","WBK","WBE" configurations, Function can be released if BT Function disabled Always exposed	1.8V; PU 100K	SOC.AE20
P56	no QSPI	SPI1_CK / ESPI_CK / QSPI_CK	ECSPI2_SCLK (GPIO5_IO10)	5	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH21
P58	no QSPI	SPI1_DO / ESPI_IO_0 / QSPI_IO_0	ECSPI2_MOSI (GPIO5_IO11)	5	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ21
P57	no QSPI	SPI1_DIN / ESPI_IO_1 / QSPI_IO_1	ECSPI2_MISO (GPIO5_IO12)	5	Available in SOM without "QSPI" configuration;	1.8V	SOC.AH20
P54	no QSPI	SPI1_CS0# / ESPI_CS0# / QSPI_CS0#	ECSPI2_SS0 (GPIO5_IO13)	5	Available in SOM without "QSPI" configuration;	1.8V	SOC.AJ22
P44		SPI0_CK	I2C1_SCL(GPIO5_IO14)	5		1.8V	SOC.AC8
P46		SPI0_DO	I2C1_SDA(GPIO5_IO15)	5		1.8V	SOC.AH7
P45		SPI0_DIN	I2C2_SCL(GPIO5_IO16)	5		1.8V	SOC.AH6

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P43	no WBE	SPI0_CS0#	I2C2_SDA(GPIO5_IO17)	5	Available in SOM without "WBE" configuration;	1.8V	SOC.AE8
S5		I2C_CAM0_CK / CSI0_TX+	I2C3_SCL(GPIO5_IO18)	5		1.8V; PU 2.2K	SOC.AJ7
S7		I2C_CAM0_DAT / CSI0_TX-	I2C3_SDA(GPIO5_IO19)	5		1.8V; PU 2.2K	SOC.AJ6
S48		I2C_GP_CK	I2C4_SCL (GPIO5_IO20)	5	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AF8
S49		I2C_GP_DAT	I2C4_SDA (GPIO5_IO21)	5	Used internally by on-SOM GP EEPROM	1.8V; PU 2.2K	SOC.AD8
P130		SER0_RX	UART1_RXD (GPIO5_IO22)	5		1.8V; PU 100K	SOC.AD6
P129		SER0_TX	UART1_TXD (GPIO5_IO23)	5		1.8V	SOC.AJ3
P135		SER1_RX	UART2_RXD (GPIO5_IO24)	5	Used as debug UART on Variscite base board	1.8V; PU 100K	SOC.AF6
P134		SER1_TX	UART2_TXD (GPIO5_IO25)	5	Used as debug UART on Variscite base board	1.8V	SOC.AH4
P131		SER0_RTS#	UART3_RXD(GPIO5_IO26)	5		1.8V	SOC.AE6
P132		SER0_CTS#	UART3_TXD(GPIO5_IO27)	5		1.8V; PU 100K	SOC.AJ4
P141		SER3_RX	UART4_RXD (GPIO5_IO28)	5		1.8V; PU 100K	SOC.AJ5
P140		SER3_TX	UART4_TXD (GPIO5_IO29)	5		1.8V	SOC.AH5

8.20 Not Connected Pins

Table 81: Not Connected Pins

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P28	no ETH_INT	GBE0_CTREF	NC	0	In "no ETH_INT" configuration this pin is Not Connected;		NC
P48		SATA_TX+	NC	0			NC
P49		SATA_TX-	NC	0			NC
P51		SATA_RX+	NC	0			NC
P52		SATA_RX-	NC	0			NC
P65	no HUB	USB1+	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
P66	no HUB	USB1-	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
P67	no HUB	USB1_EN_OC#	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
P72		RSVD	NC	0			NC
P73		RSVD	NC	0			NC
P74	no HUB	USB3_EN_OC#	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
P76	no HUB	USB4_EN_OC#	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
P77		PCIE_B_CKREQ#	NC	0			NC
P80	no COEX & BTRST	PCIE_C_REFCK+	NC	0	In "no COEX and BTRST" configuration this pin is Not Connected;		NC
P81	no COEX & BTRST	PCIE_C_REFCK-	NC	0	In "no COEX and BTRST" configuration this pin is Not Connected;		NC

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P107		DP1_AUX_SEL	NC	0			NC
S4		RSVD	NC	0			NC
S17	no EC2	GBE1_MDI0+	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S18	no EC2	GBE1_MDI0-	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S19	no EC2	GBE1_LINK_MID#	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S20	no EC2	GBE1_MDI1+	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S21	no EC2	GBE1_MDI1-	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S22	no EC2	GBE1_LINK_MAX#	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S23	no EC2	GBE1_MDI2+	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S24	no EC2	GBE1_MDI2-	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S26	no EC2	GBE1_MDI3+	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S27	no EC2	GBE1_MDI3-	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S28	no ETH_INT	GBE1_CTREF	NC	0	In "no ETH_INT" configuration this pin is Not Connected;		NC
S29		PCIE_D_TX+ / SERDES_0_TX+	NC	0			NC
S30		PCIE_D_TX- / SERDES_0_TX-	NC	0			NC
S31	no EC2	GBE1_LINK_ACT#	NC	0	In "no EC2" configuration this pin is Not connected;		NC
S32		PCIE_D_RX+ / SERDES_0_RX+	NC	0			NC
S33		PCIE_D_RX- / SERDES_0_RX-	NC	0			NC
S35	no HUB	USB4+	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S36	no HUB	USB4-	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S37		USB3_VBUS_DET	NC	0			NC
S43	no AC & no SAI3	ESPI_ALERT0#	NC	0			NC
S44	no AC & no SAI3	ESPI_ALERT1#	NC	0			NC
S54	EC1	SATA_ACT#	NC	0	In "EC1" configuration this pin is Not Connected;		NC
S55		USB5_EN_OC#	NC	0			NC
S56	no QSPI	ESPI_IO_2 / QSPI_IO_2	NC	0	In "no QSPI" configuration this pin is Not Connected;		NC
S57	no QSPI	ESPI_IO_3 / QSPI_IO_3	NC	0	In "no QSPI" configuration this pin is Not Connected;		NC
S58	no AC & no SAI3	ESPI_RESET#	NC	0			NC
S59		USB5+	NC	0			NC
S60		USB5-	NC	0			NC
S62	no HUB	USB3_SSTX+	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S63	no HUB	USB3_SSTX-	NC	0	In "no HUB" configuration this pin is Not Connected;		NC

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S65	no HUB	USB3_SSRX+	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S66	no HUB	USB3_SSRX-	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S68	no HUB	USB3+	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S69	no HUB	USB3-	NC	0	In "no HUB" configuration this pin is Not Connected;		NC
S76		PCIE_B_RST#	NC	0			NC
S77	no WRST	PCIE_C_RST#	NC	0	In "no WRST" configuration this pin is Not Connected;		NC
S78		PCIE_C_RX+ / SERDES_1_RX+	NC	0			NC
S79		PCIE_C_RX- / SERDES_1_RX-	NC	0			NC
S81	COEX & no BTRST	PCIE_C_TX+ / SERDES_1_TX+	NC	0	In "COEX and no BTRST" configuration this pin is Not Connected;		
S82	COEX & no BTRST	PCIE_C_TX- / SERDES_1_TX-	NC	0	In "COEX and no BTRST" configuration this pin is Not Connected;		NC
S84		PCIE_B_REFCK+	NC	0			NC
S85		PCIE_B_REFCK-	NC	0			NC
S87		PCIE_B_RX+	NC	0			NC
S88		PCIE_B_RX-	NC	0			NC
S90		PCIE_B_TX+	NC	0			NC
S91		PCIE_B_TX-	NC	0			NC
S93	DSI2LV	DP0_LANE0+	NC	0			NC
S94	DSI2LV	DP0_LANE0-	NC	0			NC
S95		DP0_AUX_SEL	NC	0			NC
S96	DSI2LV	DP0_LANE1+	NC	0			NC
S97	DSI2LV	DP0_LANE1-	NC	0			NC
S98		DP0_HPD	NC	0			NC
S99	DSI2LV	DP0_LANE2+	NC	0			NC
S100	DSI2LV	DP0_LANE2-	NC	0			NC
S102	DSI2LV	DP0_LANE3+	NC	0			NC
S103	DSI2LV	DP0_LANE3-	NC	0			NC
S104		USB3_OTG_ID	NC	0			NC
S105	DSI2LV	DP0_AUX+	NC	0			NC
S106	DSI2LV	DP0_AUX-	NC	0			NC
S113	no WAKE	eDP1_HPD / DSI1_TE	NC	0	In "no WAKE" configuration this pin is Not Connected;		NC
S144		eDP0_HPD / DSI0_TE	NC	0			NC

8.21 Power

8.21.1 Power – SMARC Power pinout

Table 82: Power - SMARC Power pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P147		VDD_IN	VDD_IN	0	SOM Power;		VDD_IN
P148		VDD_IN	VDD_IN	0	SOM Power;		VDD_IN
P149		VDD_IN	VDD_IN	0	SOM Power;		VDD_IN
P150		VDD_IN	VDD_IN	0	SOM Power;		VDD_IN
P151		VDD_IN	VDD_IN	0	SOM Power;		VCC_SOM
P152		VDD_IN	VDD_IN	0	SOM Power;		VCC_SOM
P153		VDD_IN	VDD_IN	0	SOM Power;		VCC_SOM
S147		VDD_RTC	VBAT_RTC	0	RTC Power input;	1.2V-5.5V	VDD_RTC
P63		USB0_VBUS_DET	USB1_VBUS	0	Soc USB1 - USB0 VBUS;	5V	SOC.A11

8.21.2 Ground – SMARC Ground pinout

Table 83: Digital Ground Pins – SMARC Ground pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P2		GND	GND	0	Digital Ground;		GND
P9		GND	GND	0	Digital Ground;		GND
P12		GND	GND	0	Digital Ground;		GND
P15		GND	GND	0	Digital Ground;		GND
P18		GND	GND	0	Digital Ground;		GND
P32		GND	GND	0	Digital Ground;		GND
P38		GND	GND	0	Digital Ground;		GND
P47		GND	GND	0	Digital Ground;		GND
P50	no AC	GND	GND	0	Available in SOM without "AC" configuration;		GND
P53		GND	GND	0	Digital Ground;		GND
P53		GND	GND	0	Digital Ground;		GND
P59		GND	GND	0	Digital Ground;		GND
P68		GND	GND	0	Digital Ground;		GND
P79		GND	GND	0	Digital Ground;		GND
P82		GND	GND	0	Digital Ground;		GND
P85		GND	GND	0	Digital Ground;		GND
P88		GND	GND	0	Digital Ground;		GND
P91		GND	GND	0	Digital Ground;		GND
P94		GND	GND	0	Digital Ground;		GND
P97		GND	GND	0	Digital Ground;		GND
P100		GND	GND	0	Digital Ground;		GND
P103		GND	GND	0	Digital Ground;		GND
P120		GND	GND	0	Digital Ground;		GND
P133		GND	GND	0	Digital Ground;		GND

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P142		GND	GND	0	Digital Ground;		GND
S3		GND	GND	0	Digital Ground;		GND
S10		GND	GND	0	Digital Ground;		GND
S13		GND	GND	0	Digital Ground;		GND
S16		GND	GND	0	Digital Ground;		GND
S25		GND	GND	0	Digital Ground;		GND
S34		GND	GND	0	Digital Ground;		GND
S47		GND	GND	0	Digital Ground;		GND
S61		GND	GND	0	Digital Ground;		GND
S64		GND	GND	0	Digital Ground;		GND
S67		GND	GND	0	Digital Ground;		GND
S70		GND	GND	0	Digital Ground;		GND
S73		GND	GND	0	Digital Ground;		GND
S80		GND	GND	0	Digital Ground;		GND
S83		GND	GND	0	Digital Ground;		GND
S86		GND	GND	0	Digital Ground;		GND
S89		GND	GND	0	Digital Ground;		GND
S92		GND	GND	0	Digital Ground;		GND
S101		GND	GND	0	Digital Ground;		GND
S110		GND	GND	0	Digital Ground;		GND
S119		GND	GND	0	Digital Ground;		GND
S124		GND	GND	0	Digital Ground;		GND
S130		GND	GND	0	Digital Ground;		GND
S136		GND	GND	0	Digital Ground;		GND
S143		GND	GND	0	Digital Ground;		GND
S158		GND	GND	0	Digital Ground;		GND

8.22 Management

8.22.1 General System Management Signals – SMARC pinout

Table 84: General System Management Signals – SMARC pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P1		SMB_ALERT#	SAI1_TXD7(GPIO4_IO19)	5		1.8V; PU 2.2K	SOC.AJ13
P126		RESET_OUT#	POR_B	0		1.8V; PU 10K	SOC.J29
P127		RESET_IN#	PMIC_RST_B	0	SOM reset input pin. Internally pulled up. Once it is asserted low, SOM performs reset.	1.8V, Input via diode; PU 10K	PCA9450C HNY.8 via diode; J1.8
P128		POWER_BTN#	ONOFF	0		1.8V; PU 10K	SOC.G22
S145		WDT_TIME_OUT#	WDOG_B	0		1.8V	SOC.B6
S148		LID#	SAI1_TXD6(GPIO4_IO18)	5		1.8V; PU 10K	SOC.AC12
S149		SLEEP#	SAI1_RXFS(GPIO4_IO00)	5		1.8V; PU 10K	SOC.AJ9
S150		VIN_PWR_BAD#	PMIC_ON_REQ (via diode)	0		1.8V to VDD_IN, Input via diode; PU 100K	PCA9450C HNY.39 via diode;
S151	CHG	CHARGING#	SAI2_RXFS(GPIO4_IO21)	5	Available in SOM with "CHG" configuration; Duplicate pin on S123;	1.8V; PU 10K	SOC.AH17
S152	CHG	CHARGER_PRSNT#	SAI2_RXC(GPIO4_IO22)	5	Available in SOM with "CHG" configuration; Duplicate pin on S142;	1.8V; PU 10K	SOC.AJ16
S153		CARRIER_STBY#	PMIC_STBY_REQ_B	0	PMIC_STBY_REQ (Via inverting FET);	1.8V	SOC.J24 (Via inv. FET)
S154		CARRIER_PWR_ON	CARRIER_PWR_ON	0	SOM Peripherals' 3.3v rail Output Via resistor divider;	1.8V	SOM_3V3_PER (Via res. divider)
S155		FORCE_RECOV#	FORCE_RECOV#	0	Boot device to be rewritten / restored from an external USB Host on Module USB0, implemented with internal logic;	1.8V; PU 10K	
S156	CHG	BATLOW#	GPIO1_IO06	0	Available in SOM with "CHG" configuration; Duplicate pin on P119;	1.8V; PU 10K	SOC.A3
S157		TEST#	JTAG_MOD	0		1.8V	SOC.G20

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8.22.2   Boot configuration

The SMARC specification defines 3x BOOT_SEL and FORCE_RECOV signals which determine the boot configuration.

Table 85: Boot signals – SMARC BOOT_SEL & FORCE_RECOV pinout

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
P123		BOOT_SEL0#	BOOT_SEL0#	0	boot select signal, implemented with internal logic;	1.8V; PU 10K	P123
P124		BOOT_SEL1#	BOOT_SEL1#	0	boot select signal, implemented with internal logic;	1.8V; PU 10K	P124
P125		BOOT_SEL2#	BOOT_SEL2#	0	boot select signal, implemented with internal logic;	1.8V; PU 10K	P125
S155		FORCE_RECOV#	FORCE_RECOV#	0	Boot device to be rewritten / restored from an external USB Host on Module USB0, implemented with internal logic;	1.8V; PU 10K	S155

The VAR-SMARC-MX8M-PLUS has internal logic manipulating the i.MX8M-PLUS BOOT_MODE[0:3] signals enabling it to boot from the following boot sources:

- Module - eMMC Flash memory
- Carrier board – SD Card
- Carrier board – USB Serial Download
- Carrier board – SPI [requires "SPI BOOT" assembly option]
- Carrier board – QSPI [requires "QSPI" assembly option]

The boot source is determined according to the below settings of the BOOT_SEL, FORCE_RECOV signals:

Table 86: Boot signals – SMARC BOOT_SEL & FORCE_RECOV boot mapping

FORCE_RECOV#	BOOT_SEL2#	BOOT_SEL1#	BOOT_SEL0#	
Float	0	0	0	QSPI [default boot mode - SPI NOR 3B Read, Other boot QSPI modes can be supported via Assy option. For further support, contact sales@variscite.com]
Float	0	0	Float	Carrier SD Card
Float	0	Float	Float	Carrier SPI
Float	Float	Float	0	Module eMMC Flash
0	Float	Float	Float	USB Serial Download

In addition, the BOOT_MODE[4:5] signals of the i.MX8M-PLUS are also routed externally to Proprietary SOM pinout (Non-SMARC).

Table 87: BOOT_MODE[4:5] signals – Proprietary SOM pinout (Non-SMARC)

Pin	Assy	SMARC pin name	SOM Pin name (function)	ALT	Notes	I/O Level; PU/PD	Ball
S40		I2S0_SDOUT	SAI2_TXD(SRC_BOOT_MODE4)	6		1.8V	SOC.AH16
S51	no AC	I2S2_SDOUT / HDA_SDO / SNDW_DAT1	SAI3_TXD(SRC_BOOT_MODE5)	6	Available in SOM without "AC" configuration;	1.8V	SOC.AH18

9.   Assembly Options

To make the solution as Flexible as possible the following assembly options were added.
The assembly options help customers to order the SOM variant that includes only the needed interfaces with a lower cost.

9.1   Ethernet PHY

The SOM can be ordered without Ethernet PHY chips EC1/EC2 assembled; This allows reducing the overall cost of the product in case the Ethernet Interfaces are not used.
When EC1 is not assembled, SoC balls are exported to SOM connector instead of SMARC GBE0 interface pins and unused SMARC pins.

9.2   Analog Audio Codec

The SOM can be ordered without Audio Codec chip assembled. This allows reducing the overall cost of the product in case the Analog Audio Codec is not used.
When not assembled, SoC balls are exported to SOM connector on SMARC I2S2 interface pins.

9.3   WBD/WBK/WBE - Dual band Wi-Fi and BT/BLE, 802.15.4 combo

The SOM can be ordered without the Dual band Wi-Fi and BT/BLE, 802.15.4 combo chip assembled, it allows reducing the overall cost of the product in case the Wi-Fi and BT/BLE is not used.

9.4   USB HUB

The SOM can be ordered without USB HUB chip assembled; it allows reducing the overall cost of the product in case the additional USB HUB ports are not used.
When HUB is not assembled, USB2 SoC balls are exported to SOM connector instead of SMARC USB2 interface pins.

9.5 DSI2LV

By default, DSI is exported on SMARC DP0 pins.
In DSI2LV assembly, DSI will be exported on LVDS0 pins.

Table 88: DSI2LV assembly option

Pin #	Default SOM option (no DSI2LV)		Special SOM option (DSI2LV)	
	Pin Function	Ball	Pin Function	Ball
S93	MIPI_DSI1_D0_P	SOC.A16	NC	NC
S94	MIPI_DSI1_D0_N	SOC.B16	NC	NC
S96	MIPI_DSI1_D1_P	SOC.A17	NC	NC
S97	MIPI_DSI1_D1_N	SOC.B17	NC	NC
S99	MIPI_DSI1_D2_P	SOC.A19	NC	NC
S100	MIPI_DSI1_D2_N	SOC.B19	NC	NC
S102	MIPI_DSI1_D3_P	SOC.A20	NC	NC
S103	MIPI_DSI1_D3_N	SOC.B20	NC	NC
S105	MIPI_DSI1_CLK_P	SOC.A18	NC	NC
S106	MIPI_DSI1_CLK_N	SOC.B18	NC	NC
S125	LVDS0_D0_P	SOC.D29	MIPI_DSI1_D0_P	SOC.A16
S126	LVDS0_D0_N	SOC.E28	MIPI_DSI1_D0_N	SOC.B16
S128	LVDS0_D1_P	SOC.E29	MIPI_DSI1_D1_P	SOC.A17
S129	LVDS0_D1_N	SOC.F28	MIPI_DSI1_D1_N	SOC.B17
S131	LVDS0_D2_P	SOC.G29	MIPI_DSI1_D2_P	SOC.A19
S132	LVDS0_D2_N	SOC.H28	MIPI_DSI1_D2_N	SOC.B19
S134	LVDS0_CLK_P	SOC.F29	MIPI_DSI1_CLK_P	SOC.A18
S135	LVDS0_CLK_N	SOC.G28	MIPI_DSI1_CLK_N	SOC.B18
S137	LVDS0_D3_P	SOC.H29	MIPI_DSI1_D3_P	SOC.A20
S138	LVDS0_D3_N	SOC.J28	MIPI_DSI1_D3_N	SOC.B20

9.6 TPMST/TPMIF

The VAR-SMARC-MX8M-PLUS can be ordered with a Trusted Platform Module (TPM) 2.0:

In "TPMST" - STMicroelectronics P/N: ST33KTPM2I3WBZB1 is assembled.
In "TPMIF" - Infineon Technologies P/N: SLB9673XU20FW2613XTMA1 is assembled.

9.7 BTPCM

In case of WBD/WBK/WBE assembly, the SOM can be ordered with SAI5 balls internally connected to Bluetooth PCM lines.

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.8   COEX, BTRST

By default, COEX pins, BT, 802.15.4 Reset signals are multiplexed with SoC MIPI CSI1 2x upper data lanes. In case of WBD/WBK/WBE assembly, Wi-Fi COEX pins and BT, 802.15.4 Reset signals can be exported instead of SMARC CSI0 signals.
If choosing "COEX" and/or "BTRST" assembly option, SMARC CSI0 2x upper data lanes will not be available.

Table 89: COEX, BTRST assembly option

Pin #	Default SOM option (no COEX, no BTRST)		Special SOM option (COEX, no BTRST)		Special SOM option (no COEX, BTRST)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
P80	MIPI_CSI1_D2_P	SOC.D24	COEX_SIN_1V8	LBES5PL2xL.69	NC	NC
P81	MIPI_CSI1_D2_N	SOC.E24	COEX_SOUT_1V8	LBES5PL2xL.70	NC	NC
S81	MIPI_CSI1_D3_P	SOC.D26	NC	NC	LR_KILL_1V8	LBES5PL2xL.38
S82	MIPI_CSI1_D3_N	SOC.E26	NC	NC	BT_KILL_1V8	LBES5PL2xL.64

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.9   WRST

In case of WBD/WBK/WBE assembly, Wi-Fi Reset signal can be exported instead of unused SMARC pin.

Table 90: WRST assembly option

Pin #	Default SOM option (no WRST)		Special SOM option (WRST)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
S77	NC	NC	WB_KILL_1V8	LBES5PL2xL.63

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.10 WAKE

In case of WBD/WBK/WBE assembly, Wi-Fi/BT wakeup signals can be exported instead of unused SMARC pins.

Table 91: WAKE assembly option

Pin #	Default SOM option (no WAKE)		Special SOM option (WAKE)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
S107	NC	NC	WIFI_HOST_WAKE_1V8	LBES5PL2xL.73
S113	NC	NC	BT_DEV_WAKE_1V8	LBES5PL2xL.75
S116	NC	NC	BT_HOST_WAKE_1V8	LBES5PL2xL.76

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.11 ANT2

In case of WBD/WBK/WBE assembly, The SOM can be ordered with Dual antennas. ANT1 for Wi-Fi, ANT2 for BT and 802.15.4

Note: This assembly option was not fully tested yet; for further support, please contact sales@variscite.com

9.12 QSPI

The SOM can be ordered with QSPIA signals exported to SMARC ESPI pins instead of SPI1 interface signals and unused SMARC pins.

Table 92: QSPI assembly option

Pin #	Default SOM option (no QSPI)		Special SOM option (QSPI)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
P54	ECSPI2_SS0	SOC.AJ22	NAND_CE0_B(QSPI_A_SS0_B)	SOC.L26
P56	ECSPI2_SCLK	SOC.AH21	NAND_ALE(QSPI_A_SCLK)	SOC.N25
P57	ECSPI2_MISO	SOC.AH20	NAND_DATA01(QSPI_A_DATA1)	SOC.L25
P58	ECSPI2_MOSI	SOC.AJ21	NAND_DATA00(QSPI_A_DATA0)	SOC.R25
S56	NC	NC	NAND_DATA02(QSPI_A_DATA2)	SOC.L24
S57	NC	NC	NAND_DATA03(QSPI_A_DATA3)	SOC.N24

9.13 SAI3

In case of a SOM without Audio Codec, SAI3 I/F signals can be exported to SOM connector instead of Audio Codec signals on unused SMARC pins.

Table 93: SAI3 assembly option

Pin #	Default SOM option (no AC, no SAI3)		Special SOM option (no AC & SAI3)		Special SOM option (AC & no SAI3)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
S43	NC	NC	SAI3_RXFS(SAI3_RX_SYNC)	SOC.AJ19	DMIC_CLK	WM8904.1
S44	NC	NC	SAI3_RXC(SAI3_RX_BCLK)	SOC.AJ18	DMIC_DATA	WM8904.27
S58	NC	NC	SAI3_MCLK	SOC.AJ20	HPOUTFB	WM8904.14

9.14 CHG

In case of a Battery Charger is used externally, "CHG" assembly option can be ordered in which SoC GPIOs (exported through other SOM pins) will be exported also to the SMARC specification allocated Charger control pins.

Table 94: CHG assembly option

Pin #	Default SOM option (no CHG)		Special SOM option (CHG)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
S151	NC	NC	SAI2_RXFS(GPIO4_IO21)	SOC.AH17
S152	NC	NC	SAI2_RXC(GPIO4_IO22)	SOC.AJ16
S156	NC	NC	GPIO1_IO06	SOC.A3

9.15 ETH_INT

In case of a SOM assembled with Ethernet PHYs EC1/EC2, the Interrupt lines can be exported to unused SMARC pins.

Table 95: ETH_INT assembly option

Pin #	Default SOM option (no ETH_INT)		Special SOM option (ETH_INT)	
	SOM Pin name (function)	Ball	SOM Pin name (function)	Ball
P28	NC	NC	ETH0_INT_IN	GBE0_DP83867IRRGZ.44
S28	NC	NC	ETH1_INT_IN	GBE1_DP83867IRRGZ.44

9.16 SPI BOOT

In case of external boot from SPI is required, SPI BOOT assembly option can be ordered adding the required logic on SOM to support booting from SPI.

9.17 LPDDR4

The SOM can be ordered with different RAM size capacities; it allows reducing the overall cost of the product in case lower RAM size is sufficient.

9.18 eMMC

The SOM can be ordered with different eMMC size capacities, it allows reducing the overall cost of the product in case lower eMMC size is sufficient.

10. Electrical Specifications

10.1 Absolute Maximum Ratings

Table 96: Absolute Maximum Ratings

Pin #	Min	Max	Units	Comments
VDD_IN	-0.3	5.5	V	
USB0_VBUS_DET	-0.3	5.25	V	
VDD_RTC	-0.5	6.5	V	
Vin/Vout input/output voltage range (GPIO Type Pins)	-0.3	OVDD+0.3	V	OVDD is the I/O supply voltage
ESD damage immunity Human Body Model (HBM)	--	+/-1000	V	JS-001-2017 Reference
ESD damage immunity Charge Device Model (CDM)	--	+/-250	V	JS-002-2018 Reference

10.2 Operating Conditions

Table 97: Operating Ranges

Parameter		Min.	Typ.	Max.	Unit
VDD_IN		4.75	5	5.25	V
USB0_VBUS_DET		4.75	5	5.25	V
VDD_RTC		1.2	3	5.5	V
GPIO Type Pins	1.8	1.65	1.8	1.95	V
	3.3	3	3.3	3.6	

10.3 Power Consumption

Table 98: VAR-SMARC-MX8M-PLUS Power Consumption

Mode	Voltage	Current	Power	Conditions
Run	5V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 ax 5GHz
Run	5V	TBD	TBD	Linux up, Wi-Fi connected and Iperf is running 802.11 n 2.4GHz
Run	5V	TBD	TBD	Linux up
FHD video playback	5V	TBD	TBD	On 800x400 LCD
Standby	5V	TBD	TBD	Memory retention mode
Off (RTC)	3V	TBD	TBD	All power rails are Off, only Internal SoC RTC is powered

Note: *The Wi-Fi module needs a power source that can provide a peak current of ~1000mA@3.3V during DPD calibration when the firmware is downloaded, even though its max continuous supply current during transmission/reception is less.*
Module calibration occurs:

- *When the Module is initially powered up.*
- *The module is reset.*
- *When the radio is initialized.*
- *Every two minutes after the radio is initialized.*

NOTE

Setup:
HW: VSC-8MPQ_1800C_4096R_32G_AC_EC1_EC2_WBD_TPMST_RTC_HUB_CT_R1.0
SW: mx8mp-yocto-scarthgap-6.6.52_2.2.0-v1.4

DISCLAIMER:
The power consumption measurements apply only to limited operation scenarios.
Actual power consumption may vary depending on the interfacing peripherals and user application modes; Users must conduct testing per their specific operation scenarios.

Depending on the specific use cases and end product system design, an appropriate thermal solution should be applied.

11. Environmental Specifications

Table 99: Environmental Specifications

Parameter	Min	Max
Commercial Operating Temperature Range	0°C	70°C
Extended Operating Temperature Range	-25°C	85°C
Industrial Operating Temperature Range	-40°C	85°C
Storage temperature	-40°C	85°C
Relative humidity (operation)	10%	90%
Relative humidity (storage)	05%	95%
Prediction Method Model: Telcordia Technologies Special Report SR-332, Issue 4 50°C, GB	> 6183 Khrs	

Note: Industrial Temperature is only based on the operating temperature grade of the SoM components. Customer should consider specific thermal design for the final product based upon the specific environmental and operational conditions.

12. Mechanical

12.1 Carrier Board Mounting

The SOM has four mounting holes for securing it to the carrier board which are plated holes and connected to GND in the size/location defined by SMARC specification.

Customers requiring a mechanical solution for mounting in harsh vibration environments can use standoffs that have M2.5 threads such as the following:

Manufacturer: **Würth Elektronik**

P/N: **9774027151R**

12.2 Thermal Management

Certain operation scenarios may prompt the use of an external heat dissipation solution.
To handle intensive applications where thermal management is required, Variscite offers a heat sink designed for the VAR-SMARC family:

Variscite PN: TBD

<div style="border:1px solid red;">

DISCLAIMER:
The implemented solution may vary depending on the device operation scenario as well as its mechanical design. Thermal solution must be evaluated.

</div>

12.3 SOM Dimensions

The SOM Module size is 82mm x 50mm according to the SMARC specification.

12.3.1 CAD Files

CAD files are available for download at http://www.variscite.com/

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15. Contact Information

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